BROOKHAVEN NATIONAL LABORATORY

U.S. ATLAS PROJECT OFFICE

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UPTON, NEW YORK 11973

September 20, 2001

Mr. James Yeck
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Dr. Thomas Kirk
Associate Laboratory Director
Brookhaven National Laboratory
Upton, NY 11973

SUBJECT: U.S. ATLAS Project Monthly Status Report for July 2001

Dear Sirs:

Attached please find Monthly Status Report No. 41 for the U.S. ATLAS Project.

Sincerely yours,

William J. Willis
U.S. ATLAS Project Manager

Distribution:

- Abolins, M.
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U.S. ATLAS

PROJECT STATUS REPORT NO. 41

REPORTING PERIOD

JULY 2001

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1. PROJECT OBJECTIVE

The U.S. ATLAS Project consists of the activities to design, supply, install and commission the U.S. portion of the ATLAS detector. The detector will become part of the Large Hadron Collider (LHC) at CERN, the European Laboratory for Particle Physics. The ATLAS detector is being designed to understand the dynamics of electroweak symmetry breaking. The U.S. ATLAS collaboration is funded jointly by the U.S. Department of Energy and the National Science Foundation.

The fundamental unanswered problem of elementary particle physics relates to the understanding of the mechanism that generates the masses of the W and Z gauge bosons and of quarks and leptons. To attack this problem, one requires an experiment that can produce a large rate of particle collisions of very high energy. The LHC will collide protons against protons every 25 ns with a center-of-mass energy of 14 TeV and a design luminosity of 10^{34} cm^{-2} s^{-1}. It will probably require a few years after turn-on to reach the full design luminosity.

The detector will have to be capable of reconstructing the interesting final states. It must be designed to fully utilize the high luminosity so that detailed studies of rare phenomena can be carried out. While the primary goal of the experiment is to determine the mechanism of electroweak symmetry breaking via the detection of Higgs bosons, supersymmetric particles or structure in the WW scattering amplitude, the new energy regime will also offer the opportunity to probe for quark substructure or discover new exotic particles. The detector must be sufficiently versatile to detect and identify the final state products of these processes. In particular, it must be capable of reconstructing the momenta and directions of quarks (hadronic jets, tagged by their flavors where possible), electrons, muons, taus, and photons, and be sensitive to energy carried off by weakly interacting particles such as neutrinos that cannot be directly detected. The ATLAS detector will have all of these capabilities.

The ATLAS detector is expected to operate for twenty or more years at the CERN LHC, observing collisions of protons, and recording more than 10^7 events per year. The critical objectives to achieve these goals are:

- Excellent photon and electron identification capability, as well as energy and directional resolution.
- Efficient charged particle track reconstruction and good momentum resolution.
- Excellent muon identification capability and momentum resolution.
- Well-understood trigger system to go from 1 GHz raw interaction rate to ~100 Hz readout rate without loss of interesting signals.
- Hermetic calorimetry coverage to allow accurate measurement of direction and magnitude of energy flow, and excellent reconstruction of missing transverse momentum.
- Efficient tagging of b-decays and b-jets.

The U.S. ATLAS cost objective is $163.75M while supplying initially the work scope described in Appendix 3 of the Project Management Plan (PMP) and, if possible, all the goals described in Appendix 2 of the PMP.

The ATLAS project was initiated in FY 1996, and is scheduled for a 10-year design and fabrication period beginning in the first quarter of FY 1996, and finishing in FY 2005. This period will be followed by operation at the LHC.

2. TECHNICAL APPROACH CHANGES

No change.

3. PROJECT MANAGER'S SUMMARY ASSESSMENT – W. Willis

In this month, we focus attention on the present state of the radiation-hard voltage regulators for the electronics of LHC experiments. In order to put adequate resources on this difficult and expensive item, CERN Management arranged for a development handled by their electronics group and carried out in European industry. The devices that come out of this effort will be used by all of the experiments, with a cost that should be much lower than that obtained by separate efforts. The full weight of CERN behind this development should lead to a priority for qualified personnel in industry and a faster and better result. There is often concern that not enough work is done in a common way, and this solution seems commendable.

This logic seems compelling, and the effort was launched several years ago. As we have monitored this process, we have reported the difficulties in achieving the required radiation tolerance specifications in prototypes and what seems to be, from the outside, an insufficient priority in the industrial partner. It was clear some months ago that the delivery would be delayed by at least one year. The Research Director understood the alarm expressed by the experiments and entered into high-level negotiations with the firm, who promised to strengthen the effort and expressed confidence that satisfactory devices would be delivered, essentially respecting the low cost promised initially. The expected delivery date, however, has extended by another half-year, to the end of 2001 at least.

The impact of this problem is probably more serious in the ATLAS Liquid Argon Front End Boards, WBS 1.3.7.1, than anywhere else in the LHC. Large numbers of these regulators are needed, mounted on a complex electronics board mounted in a confined space. The devices are really needed now, as the prototype boards near production, with full production coming soon. Work-arounds have been found to allow completion and test of the prototype boards, but a further delay would hold up the production, which needs to get started next year to keep the delivery schedule and keep costs from increasing due to inefficient use of manpower. This leads to a question within the project of use of U.S. resources to attack the problem independently. A careful study of the options suggests that the cost of the devices obtained this way would be very high compared to the favorable cost obtained by CERN, and an independent development would itself be expensive and of uncertain outcome. The cost penalty could reach $2M in this one system.

We have not initiated an independent effort. We note that the boards could be staged in part, since they are reasonably accessible, should the delays increase beyond the present estimates. We have had to invest a considerable effort in the prototype work-around, and in steps to reduce the number of regulators required. We will watch the progress of the effort by CERN and continue to stress the serious consequences of further delay.

Important progress continues to be made toward bringing the Silicon Strips, WBS 1.1.2, into production, with the key Production Readiness Review for the electronics completed and quite

favorable terms negotiated with the vendor. We are pressing to get this large radiation-hard system into production early next year. Success on this front is important to reduce the uncertainty on the final use of Contingency.

We note that we now have experience on an important element of the Muon MDT Chamber production schedule, the time taken to shift from one type of chamber to another. This step took place nearly simultaneously at the three sites, and took about five weeks, compared to the three weeks assumed in the schedule. There were some problems associated with the novelty of the procedure, so we expect that the time will be somewhat less on the average of the fourteen more change-overs. Since the production itself is somewhat faster than assumed, this schedule seems to be in good shape.

4. TECHNICAL PROGRESS - SUBSYSTEM MANGERS' SUMMARIES

1.1 Subsystem Manager's Summary Murdock Gilchriese (Lawrence Berkeley Lab.)

1.1.1 Pixels

A Conceptual Design Review of most of the pixel mechanics and a PRR for the local supports were completed in July. The production-process for the disk sectors has started. Some changes in US deliverables will result from recent design decisions to simplify the B-layer supports and to integrate the entire pixel system and beampipe on the surface.

The second sensor vendor (Tesla) has not yet been qualified. Wafers have not been delivered yet.

The submission of the first full front-end prototype IC in the IBM 0.25-micron process remains on track for September.

The layout of the flex hybrid compatible with the IBM chip was completed.

The vendor making 8" dummy wafers for bump bonding qualification studies continues to have problems and it will be August before the latest difficulties are overcome. There has been progress on wafer thinning, most recently to 125 microns, although on 6" wafers so far.

1.1.2 Silicon Strip System

The ABCD PRR was completed. Contractual negotiations with Atmel were completed on favorable terms to ATLAS. The first production wafers will arrive in mid-August and then are planned to be delivered at a rate of 100 wafers every two weeks starting in mid-October. Production test systems are operational at Santa Cruz and RAL and the system at CERN has been operational. CERN may outsource its share of wafer testing as a result of limited manpower.

Preparations for module assembly/test are ramping up but considerable work remains to complete all production tooling and develop and document production processes. Biweekly meetings with RAL have started. We are dependent on RAL for much of the tooling design and will make joint orders of some final production tooling. An LBNL engineer has been diverted from pixel mechanics to design and have fabricated other tooling/fixtures where it is possible to do so.

1.1.3 RODs

A major milestone for the RODs was completed in July. Tests of the ROD prototype at LBNL and at Cambridge (with other prototypes of the DAQ system) were successful. The layout of the "production model" RODs has started. The layout, fabrication and loading should proceed quickly (first boards by end September) since only modest design changes are required. About 10 production model boards will finally be made and these are intended to be pre-production-quality RODs for use and evaluation by the user (SCT first, then pixel) communities.

1.2 Subsystem Manager's Summary **Harold Ogren (Indiana University)**

1.2.1 Mechanics

Component systems at Hampton, Duke and Indiana continued in production during June. Hampton is now processing all the HV plates and sending the HV and tension plate kits to the Duke and Indiana assembly sites. Seven modules are completed at Indiana, seven modules completed at Duke, and ten modules are in production. Production rates for module of type 1 and type 2 are now close to scheduled rates. Type 3 is still delayed due to problems with the dimensional specifications on the HV plates. Gain tests on five type 2 modules have been carried out at Duke, and one type 1 module from Indiana will soon start gain tests at Duke. Module 2.1 is being used at University of Pennsylvania for systems tests, 1.02 is at Duke for gain tests and module 1.01 at Dubna, having been irradiated in a reactor. Wire joint irradiation tests are being readied at Duke, and cooling plate tests are in progress at Indiana.

1.2.5 Electronics:

ASDBLRs:

The new "properly processed" wafers arrived in mid July and plastic packaged parts were delivered on the 31st. Preliminary measurements indicate that matching and other functionality is as expected (hoped), however, the noise measurements are not as good as the SPice simulations would have indicated. Further measurements were made on the "known bad" die and threshold matching is very good, response is slightly improved (as expected) and all functionality is ok. The tentative yield (very low statistics) now has no hit from parametric tests and so is much better than previously - nearly at the 90% level we might have expected from a MAXIM run. However, noise measurements indicate an ENC of nearly 4000 e rather than the Spice indicated 2100 e that was expected. Further work is necessary to identify the cause and to design a proper response.

DTMROCs

Eight "Good" wafers of DTMROCs (and ASDBLRs) version 00 were delivered to Penn in early July. Five wafers have been sent out for packaging in TQFPs. When those DTMROC devices return they will be run through automatic testing to determine yield and then good devices will be sent to CERN for inclusion on End Cap boards for system testing. For barrel use we are relying on using FBGA packages - a preliminary design for that package will be forwarded to Signetics for comment in early August.

Stamp boards:

The ten barrel stamp boards shipped from Lund in June have been tested on the IMS tester and then "glop topped" to protect the bonding wires to the ASDBLRs. The initial yield is high, but the boards have no input protection installed and so there have been some channel casualties. Nevertheless, we have managed to get single stamp boards reading out through the miniRod/TTC system and have managed to get the same boards reading out through the module 2 snake cable and full length (10 meter) twisted pair cable. The next step is to get several stamp boards working at once on the snake cable and then assemble this to the detector and look for cosmic ray tracks.

1.3 Subsystem Manager's Summary Richard Stroynowski (Southern Methodist University)

The barrel cryostat arrived at CERN and was placed in its final installation position in Building 180. Acceptance tests found a small leak in the warm vessel weld. This leak will be repaired in August. Final offer for the LN2 refrigerator system came within 3% of the original estimate and was accepted. The production of the refrigerator components will start shortly.

Production and preparations for the installation of HV and signal feedthroughs is on schedule.

The prototypes of all new DMILL and DSM chips have now been received and tested together for their functionality on the "1/4 FEB" system. All perform well and no problems have been found. Radiation tests of the cheaper DSM chips will be done in August and September and the selection of the production technology will be made in October. Voltage regulators remain the biggest unresolved problem for the front-end electronics. The commercial radiation tolerant regulators are about a factor of 7 more expensive than those expected from the CERN led development project. Their use would increase a cost of the front-end boards by about $2M. The prototypes of the CERN voltage regulators are delayed by at least additional 6 months (on top of previous delay of one year) and the earliest delivery date is now November 2001. In order to maintain the schedule, a design effort is underway to reduce the number of regulators on the FEB and to find a solution for the prototype board which would reduce the time needed for its final evaluation before the start of production. This problem remains a top design priority.

The production of other electronics FEB components (preamps, motherboards, trigger sum boards) is on schedule but the question of what to do to minimize the impact of electrical discharges on the system of calibration resistors remains in the R&D stage.

The FCAL assembly is showing good progress. All tubes have now been placed in the FCAL-C module and the preparations for the installation of the rods have been started. The ATLAS LArg collaboration approved the Arizona proposal to modify the FCAL-A module to become mirror symmetrical to module C. This change will require minor matching modifications and may introduce a small delay in the completion of the matrix machining. Cold cables have been delivered and their acceptance tests have started.

1.4 Subsystem Manager's Summary Larry Price (Argonne National Lab.)

Construction of submodules and modules continues to hold to the planned schedule. Submodule production at the University of Chicago is complete. At the end of July 28 modules had been shipped to CERN of the total of 64. The design and associated report of the structural calculations is largely complete for the Extended Barrel saddles. The number of fiber replacements needed for each module is continuing at a small number, mostly caused by apparent damage to the fibers by the profile stuffing machine. STEP1 testing of Batch 5 PMTs was completed during July. Work was continued on preparing for the STEP 2 testing of all batches. Batch 6 arrived at the end of the month. In July 1386 3-in-1 cards passed burn-in and testing and were shipped to CERN, so that 65% of the total have been tested and shipped. Front end Mother boards are being received steadily from the fabricator, with about 55% received by month's end. Full production has been approved for the mezzanine cards holding the CERN TTCrx ASIC. ITC work is on schedule.

1.5 Subsystem Manager's Summary **Frank Taylor (MIT)**

Progress was made on several fronts during July.

CSC documentation is now complete and is in compliance with the PRR of 27/11/00. The CSC performance review was conducted on 2/6/01 during the general ATLAS BNL Meeting. The review committee feedback was positive. Materials for the first 5 chambers have been issued. CSC base chamber production should be able to start in early September.

The design of CSC front end entered a testing phase to see if the yield, cross talk and overload recovery met requirements. The ROD layout was completed at UC Irvine.

MDT chamber production of the second series started in late July at all three US sites. At this writing the BMC has completed 2 EIS1 base chambers, Michigan 3 EMS4 base chambers and Seattle 3 EMS2 base chambers. Tube production is well ahead of need at all three sites. The precision tooling setup took longer than planned - about 5 weeks versus the scheduled 3 weeks. As noted in last month's report, an unexpected upward bow in the angle combs of about 30 microns was observed after the first chamber series production at both the Michigan and Seattle sites. A better clamping system was developed and more monitoring will be conducted at the three sites although the causation of this problem is not yet understood. Zhou (Michigan) is collating the experiences of each site in order to expedite the series 3 tooling change over - scheduled for March 02.

Parts production for the MDT chamber services progressed but the installation of them has not yet ramped up to production levels and is behind schedule. Pre-production runs of the base plates of the Faraday cages were tested at Seattle, Michigan and BMC and the production released. Gas bar manufacturing continued on schedule at Seattle and the Heim tubeletts were tested at Brandeis and Michigan and found to be of superior quality.

On the MDT electronics front the ASD prototype chips were tested and found to be acceptable except for the adjustable deadtime feature that will be further investigated. A simplification of the production design of the mezzanine boards has been developed. The chamber service module (CSM) continues to evolve towards simplicity. High voltage and signal hedgehog productions are expected to start in late CY01 but the boards could be used earlier for chamber service commissioning.

The alignment H8 setup continued at CERN and is yielding useful lessons not only in the design and operation of the endcap alignment system but also the logistics and installation techniques that will be needed to implement the endcap system. Brandeis continued to supply in-plane alignment parts.

Ahlen (BU) and associates demonstrated an excellent MDT chamber resolution (68 microns) using the EIL1 module 0 cosmic ray setup at the BMC. Similar tests are being planned for an EMS5 chamber at Michigan.

A study of the neutron sensitivity of the four muon chamber technologies of ATLAS was initiated by the BNL group (Polychronakos, Tcherniatine et al.) arising from discussions at the Gaeta Muon Meeting this June.

Frustrations continued over unresolved issues concerning the endcap chamber and alignment layouts causing some work on these system integration problems by the U.S. Muon Group to be delayed.

1.6 Subsystem Manager's Summary **Robert Blair (Argonne National Lab.)**

The workshop held in early July allowed a comprehensive (although informal) review of the overall system design. The current planning indicates some slippage in the prototype schedule. This does not necessarily threaten a delay in the final documentation and test beam trials, but any additional slippage needs to be resisted.

TTC receiver cards were delivered and used at CERN for test beam running.

1.10 Technical Coordination **D. Lissauer (BNL)**

Technical Coordination Project Office Meeting:
We had a technical coordination Project Office meeting at CERN. The main points for discussion were I) Finalizing the ATLAS baseline schedule. We are still missing some information from both the systems and some of the common projects. But in general, there has been good progress and people are reporting through the PPT (Project Progress Tracking) system. II) Discussion on building up an installation database for ATLAS that will have all the information needed for installation, as well as, the Nuclear Installation Information that is needed by CERN. This information is needed in order to satisfy the European Nuclear Regulatory requirements. III) Preliminary discussion on plans and agenda for three (3) system overview reviews that will take place in October. This included mostly information that we are still missing from the systems on Schedule, and Safety concerns, etc.

Shielding and Activation Meeting:
A meeting took place with Vincent Hedberg, the Project Leader for the Shielding systems. We discussed the agenda and dates for the review for this activity. In addition, a major simplification of the Forward Shielding might be possible. There are areas where the forward shielding seems to be over-designed. We are investigating the possibility of changing the Shape to “Cylindrical” from a Cone. That will allow us to simplify the manufacturing. In addition, modification and simplification of the Borate Polly in the Inner Detector Cavity is being investigated. All these efforts are made in order to simplify construction and access and save funds without compromising the effectiveness of the shielding.

Muon Envelopes:
The Muon forward system envelopes are still evolving. There are serious conflicts between the wheels and some of the structures on the wall. Modification will be needed to the structures and to some of the big wheel structures. At least in the case of the TGC1 wheel the inner radius, will have to be changed.

U.S. ATLAS Review of TC Coordination Efforts:
A date, October 9, 2001, to review the U.S. TC activities has been set. The review will take place at CERN. As it is hard to separate the U.S. activities from the CERN activities, we will have a presentation not only on the U.S. program but the overall TC effort with emphasis on how the US is involved.

5. OPEN ITEMS BETWEEN DOE/NSF AND U.S. ATLAS

a) Financial: There is $1,901,000 of available funding residing in management reserve and $8,689,000 of undistributed budget pending approval and implementation of MOU documents. Table 7-2 contains the summary of FY01 funds distribution. There was $800,000 requested in additional funding allocations during July.

b) Schedule: None.

c) Technical: None.

6. SUMMARY ASSESSMENT AND FORECAST

1. Financial Status

A total of $96,288,000 (58.8%) was authorized, held in reserve or identified as undistributed budget of the $163.75M Total Project Cost Objective. The details of the overall project cost objective are presented in Table 6-1 reproduced overleaf from the U.S. ATLAS Project Plan as approved on 3/18/98 and revised to include cost changes approved through BCP #46 and BCP # 48. (BCP 47 is pending release)

The details of the reported costs and reported obligations are presented in the Table 7-1 in Section 7 of this report. In addition Table7-2 shows the cost breakdown by institution and funding source.

The relationship between budget authority/cost/obligations (including an estimate of other accrued costs and obligations) is presented in Figure 9-1 in Section 9 of this report.

The level 2 CSSR statistics are presented in section 10. Performance analysis is included for major subsystems in section 8 of this report.

2. Schedule Status

See details in Figure 11-1.

The overall schedule status report is found in section 11.

The milestone log from the PMP, including revised forecast dates, is reproduced as section 12.

3. Baseline Change Proposals

Forty seven BCPs were received through June 2001. Forty five BCP's were approved, two were withdrawn .

Table 6-1 reflects all cost BCPs through 46 and BCP 48.

TABLE 6-1: SUMMARY COST ESTIMATE

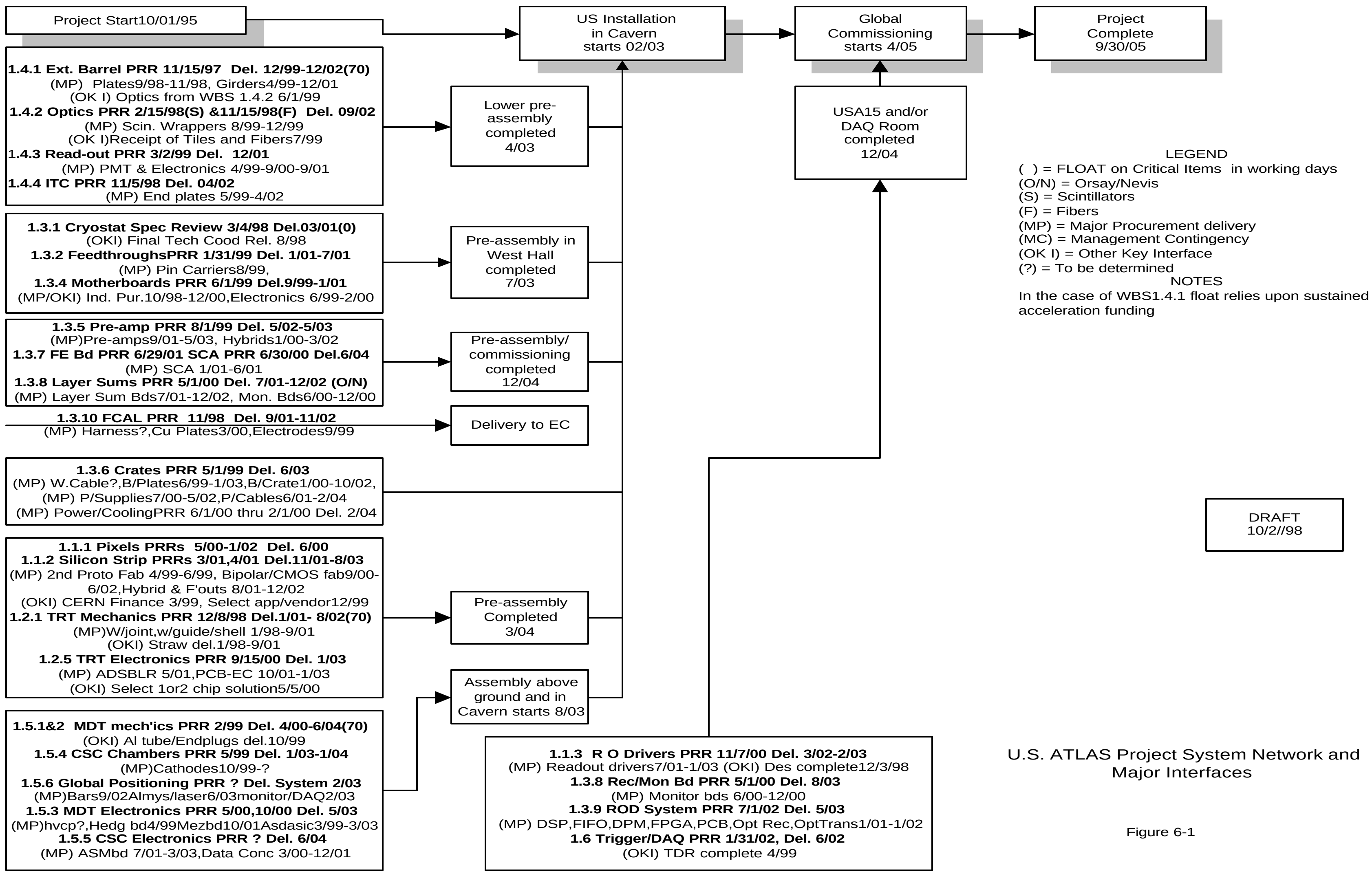
U.S.ATLAS Project
Summary Cost Estimate

Presented in (AY$ x 1000)

WBS No.	Description	Base Cost
	Technical Baseline	
1	U.S. ATLAS	
1.1	Silicon	17,795.3
1.2	TRT	9,194.0
1.3	LAr Calorimeter	42,171.6
1.4	Tile Calorimeter	9,148.2
1.5	Muon Spectrometer	26,391.2
1.7	Common Projects	9,179.1
1.8	Education	286.5
1.9	Project Management	8,279.0
1.10	Technical Coordination	450.0
	Subtotal	**122,894.9**
1.6	Trigger/DAQ Pre-Technical Baseline	3,117.9
	Subtotal	**3,117.9**
	Management Contingency	**10,451.8**
	Contingency	**19,446.0**
	Subtotal	**29,897.7**
	Technical Baseline	**155,910.5**
Items Outside of Approved Technical Baseline		
1.1.1	Pixels	-
1.6	Trigger/DAQ	**7,839.5**
	Subtotal	**7,839.5**
	Total Project Cost**	**163,750.0**

** Assumes funding profile of FY96=$1.7M, FY97=$3.7M, FY98=$10.05M,,
FY99=$25.63 FY00=$28.4M, FY01=$26.8M, FY02=$21.9M,
FY03=$25.9M,FY04=$14.7M, FY05=$5.0M.
project completion in 2005.
Includes cost changes for BCP 1-46, and 48. BCP 47 pending approval.

Figure 6-1 - Project System Network



FUNDING

Table 7.1 - Summary of Funds Authorized & Total Costs and Commitments to Date

U.S. ATLAS Project
Summary of Funds Authorized
and
Total Costs and Commitments to Date
July 31, 2001
(AY$ x 1,000)

WBS No.	Description	Funds Authorized Thru FY01	Expenses + Commitments: Expenses to Date	Open Commit	Total to Date	Balance of Authorized Funds
1.1	Silicon	12,052	8,929	82	9,011	3,041
1.2	TRT	7,217	5,055	988	6,042	1,175
1.3	LAr Calorimeter	28,014	21,428	3,874	25,302	2,712
1.4	Tile Calorimeter	8,800	7,151	119	7,270	1,530
1.5	Muon Spectrometer	16,953	12,755	1,440	14,195	2,758
1.6	Trigger/DAQ	1,977	1,655	1	1,656	321
1.7	Common Projects	5,300	5,132	-	5,132	168
1.8	Education	49	47	-	47	2
1.9	Project Management	4,886	4,418	-	4,418	468
1.10	Technical Coordination	450	106		106	344
	Subtotal	85,698	66,676	6,503	73,179	12,519
	Management Reserve	1,901			-	1,901
	Contingency	-			-	-
	Subtotal	87,599	66,676	6,503	73,179	14,420
	Undistributed Budget	8,689			-	8,689
1	U.S. ATLAS Total AY$	96,288	66,676	6,503	73,179	23,109

Table 7.2 – FY01 Funds – U.S. ATLAS Summary by Institution and Subsystem

U.S. ATLAS

FY 01 Funds

WBS 1 U.S. ATLAS Summary

Presented in (AY$x1,000)

Status as of 07/31/01

	WBS 1.1 Silicon			WBS 1.2 TRT			WBS 1.3 Liquid Argon			WBS 1.4 Tile			WBS 1.5 Muon			WBS 1.6 Trigger/DAQ			WBS 1.7 Common Projects			WBS 1.8 Education		WBS 1.9 Proj Mgmt			WBS 1.10 Tech Coord			WBS 1 U.S. ATLAS Total FY01			
	DOE		NSF	DOE		NSF	DOE		NSF	DOE		NSF	DOE		NSF	DOE		NSF	DOE		NSF	DOE	NSF	DOE		NSF	DOE		NSF	DOE		NSF	
Institution	Grant	Contract		Grant	Contract		Grant	Contract		Grant	Contract		Grant	Contract		Grant	Contract		Grant	Contract				Grant	Contract		Grant	Contract		Grant	Contract		Total
ANL	-		-	-		-	-		-		500		-		-		72		-	-	-	-	-	-		-	-		-	-	572	-	572
BNL	-		-	-		-		1,132	-					962					-	4,000	-	-	-	-	669		-	450		-	7,213	-	7,213
LBNL		1,775	-	-		-			-										-	-	-	-	-	-			-			-	1,776	-	1,775
SUNY/Albany	-		-	-		-			-										-	-	-	-	-	-			-			-	-	-	-
Arizona			-	-		-	298	153	-										-	-	-	-	-	-			-			298	153	-	451
Boston University			-	-		-			-				155						-	-	-	-	-	-			-			155	-	-	155
Brandeis University			-	-		-			-						731				-	-	-	-	-	-			-			-	-	731	731
UC Irvine				-		-			-				-		183			83	-	-	-	-	-	-			-			-	-	266	266
UC Santa Cruz			2,702	-		-			-										-	-	-	-	-	-			-			-	-	2,702	2,702
U of Chicago			-	-		-			-			723							-	-	-	-	-	-			-			-	-	723	723
Duke University			-	501					-										-	-	-	-	-	-			-			501	-	-	501
Hampton University			-			590			-										-	-	-	-	-	-			-			-	-	590	590
Harvard University			-						-						3,882				-	-	-	-	-	-			-			-	-	3,882	3,882
U of Illinois			-						-	76									-	-	-	-	-	-			-			76	-	-	76
Indiana University			-	-	616				-										-	-	-	-	-	-			-			-	616	-	616
MIT			-						-				190	100					-	-	-	-	-	-			-			190	100	-	290
Michigan State U			-						-			-						-	-	-	-	-	-	-			-			-	-	-	-
Nevis/Columbia			-						-										-	-	-	-	-	-		103	-		-	-	-	103	103
New Mexico	-	80	-																-	-	-	-	-	-		-	-		-	-	80	-	80
North Illinois U			-																-	-	-	-	-	-		-	-		-	-	-	-	-
Ohio State University	-																													-			-
U of Michigan			-										681						-	-	-	-	-	-		-	-		-	681	-	-	681
U of Oklahoma *			49																-	-	-	-	-	-		-	-		-	-	-	49	49
U of Pennsylvania			-	679															-	-	-	-	-	-		-	-		-	679	-	-	679
U of Pittsburg			-					50	201										-	-	-	-	-	-		-	-		-	-	50	201	251
U of Rochester			-						-										-	-	-	-	-	-		-	-		-	-	-	-	-
UT- Arlington			-									584							-	-	-	-	-	-		-	-		-	-	-	584	584
Southern Methodist U			-				87												-	-	-	-	-	-		-	-		-	87	-	-	87
SUNY/Stony Brook			-						426										-	-	-	-	-	-		-	-		-	-	-	426	426
Tufts University			-						-				-						-	-	-	-	-	-		-	-		-	-	-	-	-
U of Washington			-						-						1,377				-	-	-	-	-	-		-	-		-	-	-	1,377	1,377
U of Wisconsin	1,014		-						-							98			-	-	-	-	-	-		-	-		-	1,112	-	-	1,112
Total FY01	1,014	1,855	2,751	1,180	616	590	385	1,335	627	76	500	1,308	1,027	1,062	6,174	98	72	83	-	4,000	-	-	-	-	669	103	-	450	-	3,778	10,558	11,636	25,972
Reserve			-	-		-			-	-		-					-	-		-					139	654		-	-	-	139	654	793
Contingency																									-	-		-	-	-	-	-	-
Total FY01	1,014	1,855	2,751	1,180	616	590	385	1,335	627	76	500	1,308	1,027	1,062	6,174	98	72	83	-	4,000	-	-	-	-	808	758	-	450	-	3,778	10,697	12,290	26,765

* correction of prior month record of 426 to 49

8. PERFORMANCE ANALYSIS

Status through the month of July 2001 reflects the new baseline schedules for all subsystems. The re-baseline date was established on October 1, 2000 and the Estimate to Complete 01 (ETC 01) was defined as all tasks and resources required to complete the project. All prior efforts were equated to the actual costs expended. The schedules are resource loaded to the baseline funding of $163,750K with Contingency, Management Contingency, and Items Outside of the Approved Baseline shown on separate lines and excludes all NSF R&D funds.

The CSSR in section 10 shows $66,611.8k of the work has been performed, which represents approximately 52.9 of the work authorized to date. There is an unfavorable schedule variance of ($894.0k) or 1.3% behind the plan. There is an unfavorable cost variance of $64.5k or 0.1% over spent for the work accomplished. There are outstanding commitments of $6,502.3k at this time that do not show up in the performance. This analysis will provide a breakdown of these variances into the individual subsystems and identify the specific tasks that cause these variances.

WBS 1.1 Silicon

Summary

The CSSR shows that $8,653.0k of the work has been completed which represents 48.7% of the total effort for the Silicon subsystem. There is an unfavorable schedule variance of ($317.3k) or 3.5% behind the plan and an unfavorable cost variance of ($275.7k) or 3.2% over spent for the work accomplished. There are outstanding commitments of $82.1k at this time that do not show up in the performance.

Schedule Variance

The unfavorable schedule variance is concentrated in the following WBS level 3 elements:

WBS 1.1.2 Silicon Strip System SV = ($82.4k)

- Hybrids/Cables/Fanouts are behind plan ($28.5k)
- Module Assembly and Test is behind plan ($53.9k)

WBS 1.1.3 RODs SV = ($231.6k)

- Design ROD Cards is behind plan ($9.2k)
- ROD Test Stand is behind plan ($59.3k)
- ROD Prototypes is behind plan ($51.2k)
- ROD Prototype Evaluation is behind plan ($17.4k)
- ROD Production Model is behind plan ($91.0k)
- ROD Fabrication is behind plan ($3.4k)

Cost Variance

There is a unfavorable cost variance of ($275.7k) which is distributed as follows: Pixel ($403.9k), the Silicon Strip System $283.8k and the ROD Design and Fabrication ($155.6k).

WBS 1.2 TRT

Summary

The CSSR shows that $4,970.1k of the work has been completed which represents 54.1% of the total effort for the TRT subsystem. There is an unfavorable schedule variance of ($285.7k) or 5.4% behind the plan and an unfavorable cost variance of $84.8k or 1.7% under spent for the work accomplished. There are outstanding commitments of $987.5k at this time that do not show up in the performance.

Schedule Variance

The unfavorable schedule variance is concentrated in the following WBS level 3 elements

WBS 1.2.1 Barrel Mechanics SV = ($273.2k)

- Detector Elements are behind plan ($31.6k)
- Component Assembly is behind plan ($109.9k)
- Module Assembly #2 (Duke) is behind plan ($66.3k)
- Module Assembly #1 (IU) is behind plan ($62.9k)

WBS 1.3 LAr

Summary

The CSSR shows that $22,294.7k of the work has been completed which represents 52.9% of the total effort for the LAr subsystem. There is an unfavorable schedule variance of ($123.5k) or 0.6% behind the plan and a favorable cost variance of $866.9k or 2.2% under spent for the work accomplished. There are outstanding commitments of $3,873.8k at this time that do not show up in the performance.

Schedule Variance

The unfavorable schedule variance is concentrated in the following WBS level 3 elements:

1.3.1 Barrel Cryostat SV = ($6.6k)
1.3.3 Cryogenics SV = ($27.6k)
1.3.10 Forward Calorimeter SV = ($76.4k)

- FCAL1 Module Production is behind plan ($28.2k)
- FCAL Electronics Design and Tooling are behind plan ($15.9k) and ($17.9k) respectively
- FCAL Production is behind plan ($14.3k)

Cost Variance

The favorable cost variance of $493.3k is a combination of positive and negative variances concentrated in the following WBS Level 3 elements.

- 131 Barrel Cryostat CV = $489.3k
- 132 Feedthroughs CV = ($198.4k)
- 133 Cryogenics CV = $698.9k
- 134 Readout Electrodes/MB CV = ($64.4k)
- 135 Preamp/Calibration CV = ($61.9k)
- 136 System Crate Integration CV = ($215.4k)
- 137 Front End Board CV = ($148.4k)
- 139 ROD System CV = $128.5k
- 1310 Forward Calorimeter CV = ($129.5k)

WBS 1.4 Tile

Summary

The CSSR shows that $7,246.8k of the work has been completed which represents 79.2% of the total effort for the Tile subsystem. There is an unfavorable schedule variance of ($27.2k) or 0.4% behind the plan and a favorable cost variance of $95.6k or 1.3% under spent for the work accomplished. There are outstanding commitments of $118.7k at this time that do not show up in the performance.

Schedule Variance

The unfavorable schedule variance is concentrated in the following WBS level 3 elements:

1.4.3 Readout SV = ($0)
1.4.4 Intermediate Tile Calorimeter SV = ($23.0k)

Cost Variance

There is a favorable cost variance of $95.6k which is distributed as follows:

- 141 EB Mechanics ($76.0k)
- 142 EB Optics ($56.8k)
- 143 Readout $264.5k
- 144 ITC ($36.1k)

WBS 1.5 Muon

Summary

The CSSR shows that $12,551.0k of the work has been completed which represents 47.6% of the total effort for the Muon subsystem. There is an unfavorable schedule variance of ($104.3k) or 0.8% behind the plan and an unfavorable cost variance of ($203.5k) or 1.6% over spent for the work accomplished. There are outstanding commitments of $1,440.1k at this time that do not show up in the performance.

Schedule Variance

The unfavorable schedule variance is concentrated in the following WBS level 3 elements:

1.5.7 MDT Chambers SV = ($43.8k)

- Chamber Integration Drawings ($5.7k)
- Chamber Construction ($33.6k)

1.5.8 MDT Supports SV = ($38.2k)

- Chamber Mount Struts Design is behind plan ($15.5k)
- Integration with Support Structure Design is behind plan ($20.7k)

Cost Variance

The unfavorable cost variance of ($203.5k) is a combination of positive and negative variances concentrated in the following WBS Level 3 elements.

- 154 CSC Chambers CV = 0
- 157 MDT Chambers CV = $16.8k)

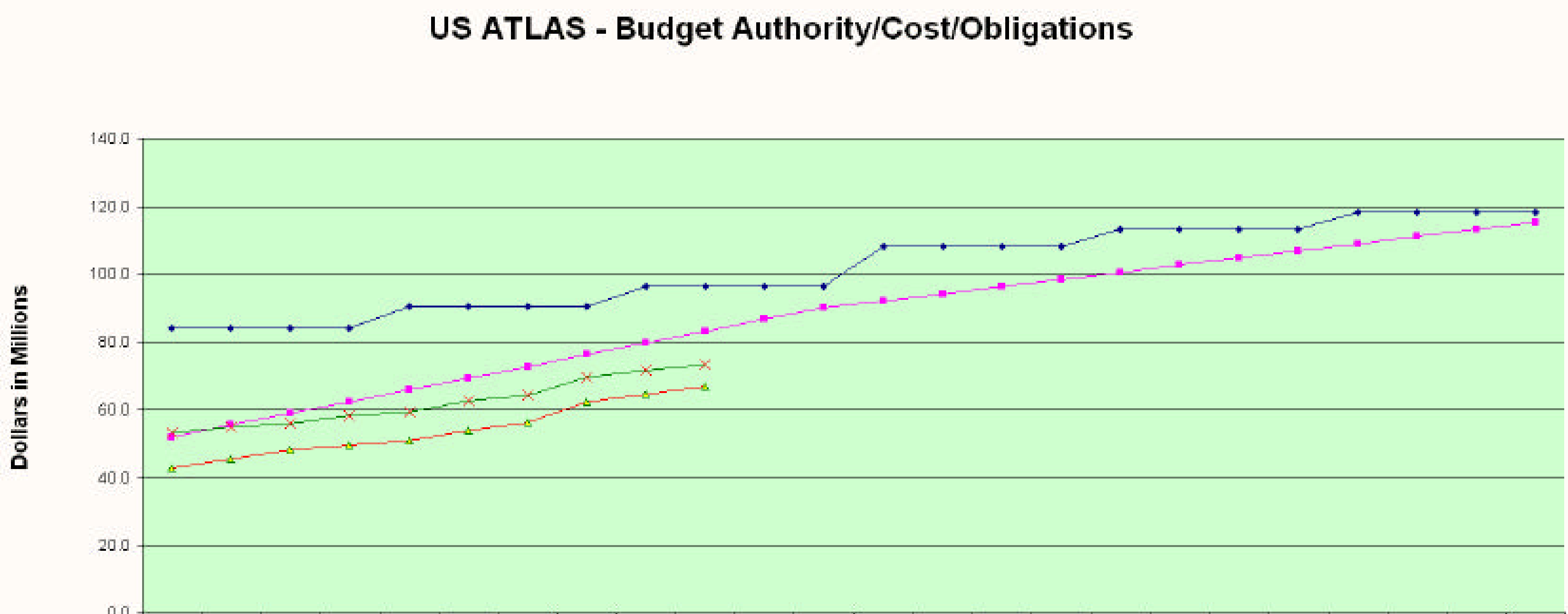
- 158 MDT Supports CV = ($36.2k)
- 159 MDT Electronics CV = $60.1k
- 1511 CSC Electronics CV = ($90.3k)
- 1512 Global Align System CV = ($153.9k)

WBS 1.6 Trigger/DAQ

Summary

The CSSR shows that $1,566.1k of the work has been completed which represents 50.2% of the total effort for the Trigger/DAQ subsystem. There is an unfavorable schedule variance of ($36.1k) or 2.3% behind the plan and an unfavorable cost variance of ($89.2k) or 5.7% over spent for the work accomplished. There are unfavorable cost variances of ($178.5k) for the Level 2 Supervisor and ($7.9k) for Architecture, but, these are offset by favorable cost variances of 89.9k for the Level 2 Calorimeter Trigger and $7.4k for the Level 2 SCT Trigger. There are outstanding commitments of $0.1k at this time that do not show up in the performance.

9. BUDGET AUTHORITY COSTS AND OBLIGATIONS



	O 00	N 00	D 00	J 01	F 01	M 01	A 01	M 01	J 01	J 01	A 01	S 01
BA CUM	84.030	84.030	84.030	84.030	90.320	90.320	90.320	90.320	96.320	96.320	96.320	96.320
Plan Cost	52.078	55.530	58.981	62.433	65.884	69.336	72.787	76.239	79.691	83.142	86.594	90.045
Cost	42.874	45.510	48.302	49.611	50.849	53.849	56.299	62.165	64.777	66.986		
Cost+Oblig	53.367	55.051	56.073	58.241	59.391	62.703	64.282	69.598	71.753	73.488		

	O 01	N 01	D 01	J 02	F 02	M 02	A 02	M 02	J 02	J 02	A 02	S 02
BA CUM	108.170	108.170	108.170	108.170	113.170	113.170	113.170	113.170	118.170	118.170	118.170	118.170
Plan Cost	92.152	94.259	96.365	98.472	100.579	102.686	104.792	106.899	109.006	111.113	113.219	115.326
Cost												
Cost+Oblig												

Month-Year

10. WBS – COST SCHEDULE STATUS REPORT

Project Status Report
Section 10

U.S. ATLAS

Cost Schedule Status Report

Reporting Period Ending:07/31/01

		Cumulative To Date (k$)					At Completion (k$)			Complete (%)		
		Budgeted Cost		Actual Cost	Variance			Latest				
		Work	Work	Of Work			Budgeted	Revised				
	WBS Element	Scheduled	Performed	Performed	Schedule	Cost	AY $s	Estimate	Variance	Scheduled	Performed	Actual
1.1	Silicon	8,970.3	8,653.0	8,928.7	(317.3)	(275.7)	17,755.1	17,755.1	-	50.5	48.7	50.3
1.2	TRT	5,255.9	4,970.1	5,054.9	(285.7)	(84.8)	9,194.0	9,194.0	0.0	57.2	54.1	55.0
1.3	Liquid Argon	22,418.2	22,294.7	21,427.8	(123.5)	866.9	42,171.6	42,171.6	0.0	53.2	52.9	50.8
1.4	TileCal	7,274.0	7,246.8	7,151.2	(27.2)	95.6	9,148.2	9,148.2	0.0	79.5	79.2	78.2
1.5	Muon	12,655.3	12,551.0	12,754.5	(104.3)	(203.5)	26,391.2	26,391.2	-	48.0	47.6	48.3
1.6	Trigger/DAQ	1,602.1	1,566.1	1,655.3	(36.1)	(89.2)	3,117.9	3,117.9	(0.0)	51.4	50.2	53.1
1.7	Common Projects [1]	5,132.2	5,132.2	5,132.2	-	-	9,179.1	9,179.1	-	55.9	55.9	55.9
1.8	Education [1]	47.2	47.2	47.2	-	-	286.5	286.5	-	16.5	16.5	16.5
1.9	Project Management [1]	4,418.1	4,418.1	4,418.1	-	-	8,279.0	8,279.0	-	53.4	53.4	53.4
1.10	Technical Coordination	106.4	106.4	106.4	-	-	450.0	450.0	-	23.6	23.6	23.6
Sub Total		67,879.6	66,985.6	66,676.3	(894.0)	309.3	125,972.6	125,972.6	0.0	53.9	53.2	52.9
Management Reserve							0.0	0.0	-			
Contingency							19,466.1	19,466.1	-			
Management Contingency							10,471.9	10,471.9	-			
Items Outside of Approved Baseline							7,839.5	7,839.5	0.0			
Escalation							0.0	0.0	-			
U.S. ATLAS Total		67,879.6	66,985.6	66,676.3	(894.0)	309.3	163,750.0	163,750.0	0.0	41.5	40.9	40.7

Notes: 1 LOE

FIGURE 11-1 - MILESTONE SCHEDULE STATUS REPORT

ID	Subsystem ID	Milestone	ETC 01 Baseline	Forecast	Actual
1		Project Start (10/1/95)	Sun 10/1/95	Sun 10/1/95	Sun 10/1/95
2	Tile L2/1	Start Submodule Procurement	Mon 9/1/97	Mon 9/1/97	Mon 9/1/97
3	Tile L2/2	Technology Choice for F/E Electronics	Sat 11/15/97	Sat 11/15/97	Sat 11/15/97
4	LAr L2/1	Cryostat Contract Award	Fri 7/24/98	Wed 8/5/98	Wed 8/5/98
5	LAr L2/2	Barrel FTs Final Design Review	Wed 9/30/98	Fri 10/2/98	Fri 10/2/98
6	TRT L2/1	Final Design Complete	Thu 12/31/98	Mon 12/7/98	Mon 12/7/98
7	LAr L2/4	FCAL Mech Design Complete	Mon 12/14/98	Wed 12/15/99	Wed 12/15/99
8	Tile L2/3	Start Module Construction	Sat 5/1/99	Mon 9/20/99	Mon 9/20/99
9	TDAQ L2/1	Select Final LVL2 Architecture	Fri 12/31/99	Fri 3/31/00	Fri 3/31/00
10	LAr L2/3	Start Elec.'s Production (Preamps)	Fri 6/30/00	Fri 6/30/00	Fri 6/30/00
11	Muon L2/1	Start MDT Chambers Lines 1 & 3	Mon 7/17/00	Fri 9/15/00	Fri 9/15/00
12	Muon L2/6	Kinematic Mount Design Complete	Tue 1/30/01	Tue 1/30/01	Tue 1/30/01
13	Tile L2/4	Start Production of MBs	Sun 4/1/01	Fri 3/30/01	Fri 3/30/01
14	LAr L2/9	Cryostat Arrives at CERN	Tue 5/15/01	Mon 7/2/01	**Mon 7/2/01**
15	TRT L2/4	Select Final Elec Design	Fri 6/15/01	Wed 8/30/00	Wed 8/30/00
16	Sil L2/1	Start Full Silicon Strip Elec Production	Fri 7/6/01	Sun 7/15/01	**Sun 7/15/01**
17	LAr L2/5	FEB SCA Prod Chip Submission/CA	Thu 7/19/01	Mon 10/1/01	NA
18	Sil L2/6	Pixels '1st IBM Prototype Submitted'	Thu 7/26/01	Mon 9/17/01	NA
19	Muon L2/2	Start CSC Chamber Production	Sat 9/1/01	Sat 9/1/01	NA
20	Sil L2/3	ROD Design Complete	Mon 10/1/01	Mon 10/1/01	NA
21	LAr L2/6	Level 1 Trigger Final Design Complete	Thu 10/4/01	Thu 10/4/01	NA
22	Muon L2/3	MDT Electronics ASD PRR	Fri 10/19/01	Fri 10/19/01	NA
23	Sil L2/2	Start Full Strip Module Production	Mon 1/7/02	Mon 1/7/02	NA
24	TRT L2/5	Start Production of ASICS	Fri 1/18/02	Fri 1/18/02	NA
25	LAr L2/10	Barrel FTs Production Complete	Fri 2/15/02	Fri 2/15/02	NA

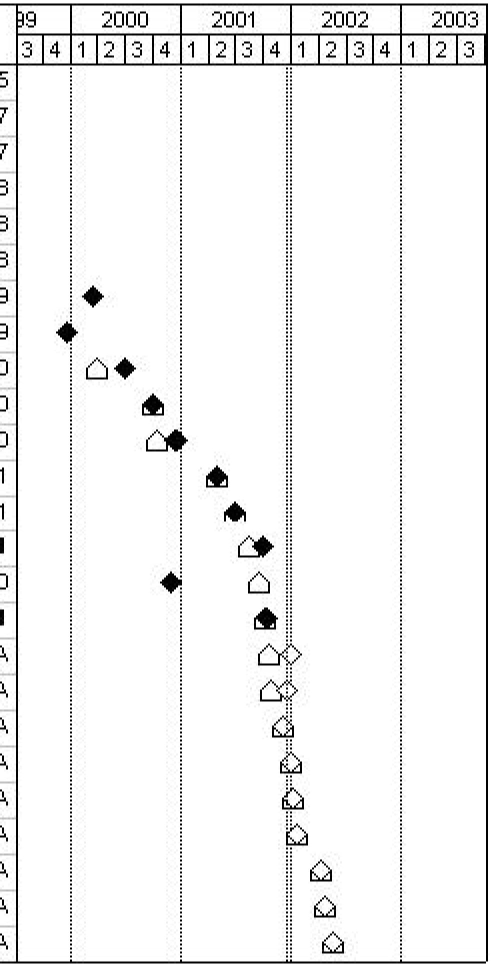
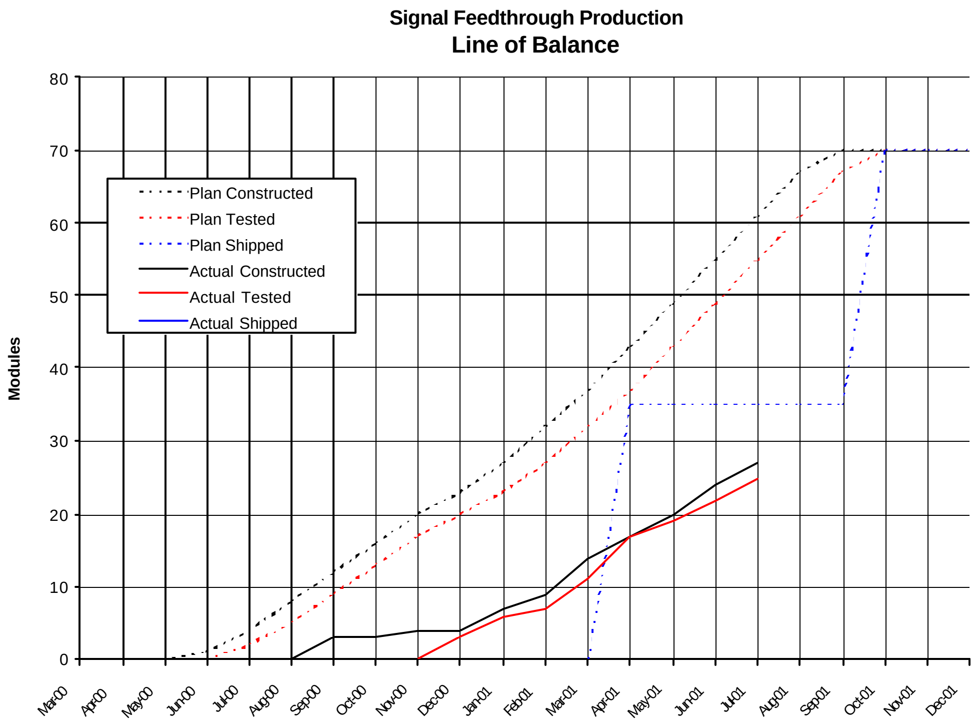
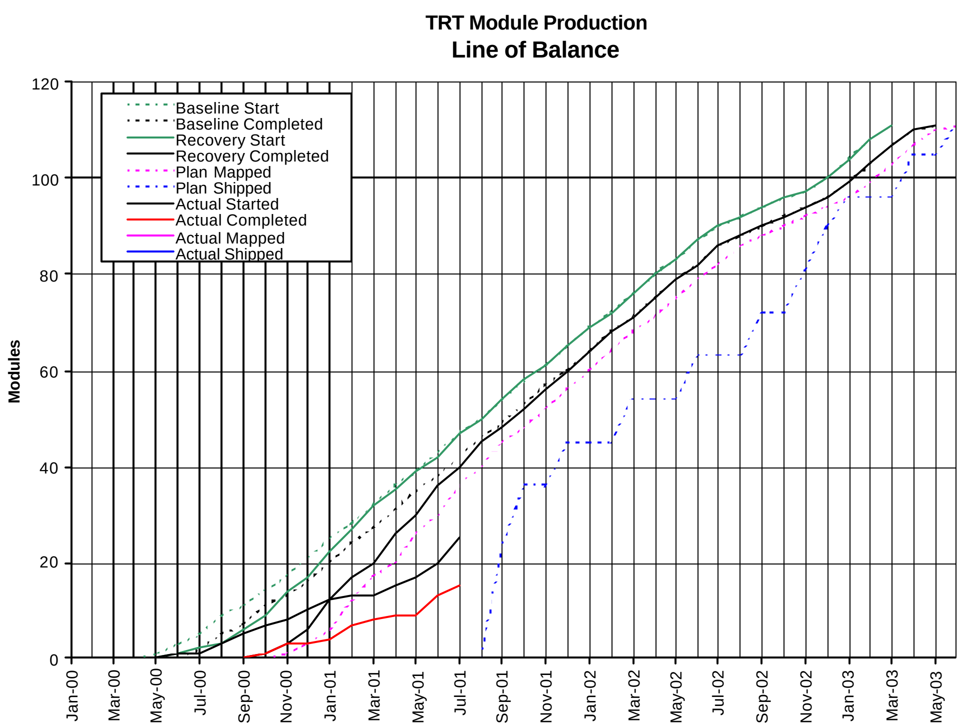


FIGURE 11-2 - LINE OF BALANCE THROUGH JUNE 2001





12. MILESTONE LOG

The milestones have been updated with the new ETC 01 baseline dates.

U.S. ATLAS Major Project Milestones (Level 1)

Description	Baseline Schedule	Forecast (F) Date	Actual (A) Date
Project Start	01-Oct-95	01-Oct-95 (F)	01-Oct-95 (A)
Project Completion	30-Sep-05	30-Sep-05 (F)	

U.S. ATLAS Major Project Milestones (Level 2)

Subsystem	**Schedule Designator**	**Description**	**Baseline Schedule**	**Forecast (F) / Actual (A) Date**
Silicon (1.1)	SIL L2/1	Start Full Silicon Strip Electronics Production	06-Jul-01	**15-Jul-01 (A)**
	SIL L2/2	Start Full Strip Module Production	07-Jan-02	07-Jan-02 (F)
	SIL L2/3	ROD Design Complete	01-Oct-01	01-Oct-01 (F)
	SIL L2/4	Complete Shipment of Silicon Strip Module Production	13-Oct-03	13-Oct-03 (F)
	SIL L2/5	ROD Production/Testing Complete	24-Jun-03	24-Jun-03 (F)
	SIL L2/6	Pixels 1st IBM Prototype Submitted	26-Jul-01	17-Sep-01 (F)
	SIL L2/7	Pixels Start IBM Production	13-Mar-03	13-Mar-03 (F)
	SIL L2/8	Pixels Start IBM Outer Bare Module Prod	22-Oct-03	22-Oct-03 (F)
	SIL L2/9	Pixels Disk System at CERN	13-Oct-04	13-Oct-04 (F)
TRT (1.2)				
Mechanical	TRT L2/1	Final Design Complete	31-Dec-98	07-Dec-98 (A)
	TRT L2/2	Module Production Complete (CUM 102)	31-Mar-03	31-Mar-03 (F)
	TRT L2/3	Barrel Construction Complete	16-Sep-03	16-Sep-03 (F)
Electrical	TRT L2/4	Select Final Elec Design	15-Jun-01	30-Aug-00 (A)
	TRT L2/5	Start Production of ASICS	18-Jan-02	18-Jan-02 (F)
	TRT L2/6	Installation Complete	04-Jan-05	04-Jan-05 (F)
LAr Cal (1.3)	LAr L2/1	Cryostat Contract Award	24-Jul-98	05-Aug-98 (A)
	LAr L2/2	Barrel Feedthroughs Final Design Review	30-Sep-98	02-Oct-98 (A)
	LAr L2/3	Start Electronics Production (Preamps)	30-Jun-00	30-Jun-00 (A)
	LAr L2/4	FCAL Mechanical Design Complete	14-Dec-98	15-Dec-99 (A)
	LAr L2/5	FEB SCA Prod. Chip Submission/Contract Award	19-Jul-01	01-Oct-01 (F)
	LAr L2/6	Level 1 Trigger Final Design Complete	04-Oct-01	04-Oct-01 (F)
	LAr L2/7	ROD Final Design Complete	12-Dec-02	12-Dec-02 (F)
	LAr L2/8	Motherboard System Production Complete	30-Jun-02	30-Jun-02 (F)
	LAr L2/9	Cryostat Arrives at CERN	15-May-01	**02-Jul-01 (A)**
	LAr L2/10	Barrel Feedthroughs Production Complete	15-Feb-02	15-Feb-02 (F)
	LAr L2/11	FCAL-C Delivered to EC	17-Oct-02	17-Oct-02 (F)
	LAr L2/12	FCAL-A Delivered to EC	08-Dec-03	08-Dec-03 (F)

Subsystem	Schedule Designator	Description	Baseline Schedule	Forecast (F) / Actual (A) Date

U.S. ATLAS Major Project Milestones (Level 2) (Continued)

Subsystem	Schedule Designator	Description	Baseline Schedule	Forecast (F) / Actual (A) Date
Tile Cal (1.4)	Tile L2/1	Start Submodule Procurement	01-Sep-97	01-Sep-97 (A)
	Tile L2/2	Technology Choice for F/E Electronics	15-Nov-97	15-Nov-97 (A)
	Tile L2/3	Start Module Construction	01-May-99	20-Sep-99 (A)
	Tile L2/4	Start Production of Motherboards	01-Apr-01	30-Mar-01 (A)
	Tile L2/5	All Electronic Components Delivered to CERN	01-Oct-02	01-Oct-02 (F)
	Tile L2/6	Module Construction Complete	30-Sept-02	30-Sep-02 (F)
	Tile L2/7	All Modules Delivered to CERN	02-Dec-02	02-Dec-02 (F)
Muon (1.5)	Muon L2/1	Start MDT Chambers Lines 1 and 3	17-Jul-00	15-Sep-00 (A)
	Muon L2/2	Start CSC Chamber Production	01-Sep-01	01-Sep-01 (F)
	Muon L2/3	MDT Electronics ASD PRR	19-Oct-01	01-Oct-01 (F)
	Muon L2/4	Final Design of Global Alignment Devices Complete	01-Apr-02	01-Apr-02 (F)
	Muon L2/5	CSC IC Production Complete	15-May-02	15-May-02 (F)
	Muon L2/6	Kinematic Mount Design Complete	30-Jan-01	30-Jan-01 (A)
	Muon L2/7	MDT Chambers (U.S.) Production Complete	27-Aug-04	14-Sep-04 (F)
	Muon L2/8	Kinematic Mount Production Complete	24-May-04	24-May-04 (F)
	Muon L2/9	CSC ROD Production Complete	05-Nov-03	05-Nov-03 (F)
	Muon L2/10	MDT Elec.'s Mezzanine Production Complete	06-Mar-03	06-Mar-03 (F)
	Muon L2/11	CSC Assembly/Testing at CERN Complete	17-Dec-04	17-Dec-04 (F)
	Muon L2/12	Global Alignment System Final Delivery	30-Sep-04	30-Sep-04 (F)
Trigger/ DAQ (1.6)	TDAQ L2/1	Select Final LVL2 Architecture	31-Dec-99	31-Mar-00 (A)
	TDAQ L2/2	LVL2 Trigger Design Complete	31-Dec-02	31-Dec-02 (F)
	TDAQ L2/3	LVL2 Trigger Prototype Complete	30-Sep-02	30-Sep-02 (F)
	TDAQ L2/4	Start Production	08-Jan-03	08-Jan-03 (F)
	TDAQ L2/5	Start Installation & Commissioning	05-Mar-03	05-Mar-03 (F)
	TDAQ L2/6	Production Complete	30-Jul-05	30-Jul-05 (F)
	TDAQ L2/7	LVL2 Installation & Commissioning Complete	30-Sep-05	30-Sep-05 (F)

U.S. ATLAS Major Project Milestones (Level 4)

WBS	Schedule Designator	U.S. ATLAS Responsibility Completion Description	ETC01 Baseline Scope Planned Completion Date	Forecast (F)/ Actual (A) Baseline Scope Completion Date	ATLAS Required Date	Baseline Scope Planned Float (Months)
Silicon						
1.1.2	Sil L4/1	Complete Shipping of Silicon Strip Prod Modules	10/03	10/03	4/03	-6
1.1.3	Sil L4/2	RODs 45% Production Complete	9/02	9/02	6/03	9
1.1.1	Sil L4/3	Pixels 'Disk System at CERN'	10/04	10/04	12/04	2
TRT						
1.2.1	TRT L4/1	Barrel Modules Ship to CERN Complete	8/02	8/02	3/03	7
1.2.5	TRT L4/2	ASDBLRs Ship to LUND Complete	10/02	10/02	11/02	1
	TRT L4/3	ASDBLRs Ship to CERN Complete	11/02	11/02	12/02	1
	TRT L4/4	PCB-Endcaps Ship to CERN Complete	4/03	4/03	10/03	6
LAr						
1.3.1	LAr L4/1	Cryostat Final Acceptance Test Complete	8/01	8/01	11/01	3
1.3.2	LAr L4/2	Signal FT Installation Complete	11/02	11/02	10/02	-1
	LAr L4/3	HV FT End-Cap C Install Complete	2/02	2/02	11/01	-3
	LAr L4/4	HV FT Barrel Install Complete	11/01	11/01	5/02	6
	LAr L4/5	HV FT End-Cap A Install Complete	12/02	12/02	9/02	-3
1.3.3	LAr L4/6	LAr Cryogenics Vendor Install Complete	9/03	9/03	12/03	3
1.3.4.1	LAr L4/7	Last Del of Readout Electrodes	12/02	12/02	10/02	-2
1.3.4.2	LAr L4/8	MBs Ship to Annecy,Saclay (France)	6/02	6/02	9/02	3
1.3.5.1	LAr L4/9	Preamp Deliveries to FEB Complete	5/03	5/03	3/04	10
1.3.5.2	LAr L4/10	Prec Calor Calib Production Complete	N/A	N/A	N/A	N/A

U.S. ATLAS Major Project Milestones (Level 4) (Continued)

WBS	Schedule Designator	U.S. ATLAS Responsibility Completion Description	ETC01 Baseline Scope Planned Completion Date	Forecast (F)/ Actual (A) Baseline Scope Completion Date	ATLAS Required Date	Baseline Scope Planned Float (Months)
Lar (Continued)						
1.3.6.1	LAr L4/12	Pedestal Ship to CERN Complete	12/01	12/01	7/02	7
	LAr L4/13	Barrel Ship to CERN Complete	12/01	12/01	3/03	15
1.3.6.2	LAr L4/14	Cables Shipping Complete	10/02	10/02	3/03	5
	LAr L4/15	Baseplane Last Delivery to CERN Complete	10/02	10/02	3/03	5
1.3.6.3	LAr L4/16	EC Crates Last Delivery to CERN Complete	10/02	10/02	3/03	5
	LAr L4/17	Barrel Crates Last Delivery to CERN Complete	10/02	10/02	3/03	5
1.3.6.4	LAr L4/18	Controls Ship to CERN Complete	9/03	9/03	5/04	8
	LAr L4/19	Power Supplies Last Delivery Complete	9/04	9/04	5/04	-4
1.3.6.5	LAr L4/21	Thermal Contacts (Proto) Last Delivery Complete	9/02	9/02	9/02	0
1.3.7.1	LAr L4/22	FEB Last Delivery Complete	8/04	8/04	1/05	5
1.3.7.2	LAr L4/23	SCAs Last Delivery to FEB Complete	N/A	N/A	N/A	N/A
1.3.7.4	LAr L4/24	Last Driver Delivery to FEB Complete	4/04	4/04	5/04	1
1.3.8.1	LAr L4/26	Layer Sums Last Delivery to FEB Complete	12/02	12/02	3/04	15
1.3.8.2	LAr L4/27	I/F to Level 1 Ship to CERN Complete	8/04	8/04	12/04	4
1.3.9	LAr L4/28	ROD System Final Prototype Complete	8/02	8/02	8/02	0
1.3.10	LAr L4/29	Deliver Finished FCAL-C to EC	10/02	10/02	10/02	0
	LAr L4/30	Deliver Finished FCAL-A to EC	12/03	12/03	11/03	-1
	LAr L4/31	FCAL Elec.'s Summ Bds Ready for Installation	12/01	12/01	2/02	2
	LAr L4/32	FCAL Elec.'s Cold Cables Testing Complete	11/01	11/01	2/02	3

U.S. ATLAS Major Project Milestones (Level 4) (Continued)

WBS	Schedule Designator	U.S. ATLAS Responsibility Completion Description	ETC01 Baseline Scope Planned Completion Date	Forecast (F)/ Actual (A) Baseline Scope Completion Date	ATLAS Required Date	Baseline Scope Planned Float (Months)
Tile						
1.4.1	Tile L4/1	Submodules Prod Compl (Original Baseline Scope)	7/01	**3/01 (A)**	8/01	**5**
	Tile L4/2	EB Module Ship to CERN Complete	12/01	12/01	7/02	7
1.4.2	Tile L4/3	Optics Instrumentation at ANL & MSU Complete	9/02	9/02	11/02	2
1.4.3	Tile L4/4	PMT Ship to ATLAS Complete	1/02	1/02	7/02	6
1.4.3	Tile L4/5	Readout Ship to ATLAS Complete	6/02	6/02	9/02	3
1.4.4	Tile L4/6	Gap Submodules Ship to ANL & BCN Compl (Original Baseline Scope)	7/01	**4/01 (A)**	8/01	**4**

Muon						
1.5.7 (1)	Muon L4/1	MDT Chamber Prod Complete (BMC Qty. 80)	6/04	6/04	2/04	-4
		MDT Chamber Prod Complete (Mich Qty. 80)	8/04	8/04	2/04	-6
		MDT Chamber Prod Complete (Seattle Qty. 80)	8/04	8/04	2/04	-6
1.5.8 (2)	Muon L4/2	MDT Mounts Prod Complete/Delivered to Chambers	10/03	10/03	2/04	4
1.5.9 (3)	Muon L4/3	MDT Elec.'s Mezzanine Bd Production Complete	3/03	3/03	2/03	-1
	Muon L4/4	MDT Elec.'s Hedgehog Production Complete	12/01	12/01	4/01	-8
1.5.4	Muon L4/5	CSC Chambers Production Complete	1/03	1/03	4/04	15
1.5.11 (5)	Muon L4/6	ASMs Production Complete	4/04	4/04	4/04	0
	Muon L4/7	Sparsifiers Ship to CERN	3/04	3/04	10/04	7
	Muon L4/8	RODs Ship to CERN	3/04	3/04	10/04	7
	Muon L4/9	Support Electronics Ship to CERN	3/04	3/04	10/04	7
1.5.12 (6)	Muon L4/10	Align Bars Ship to CERN	3/04	3/04	12/04	9
	Muon L4/11	Proximity Monitors Ship to CERN	12/03	12/03	12/04	12
	Muon L4/12	Multi-Point System Ship to CERN	3/03	3/03	3/05	24
	Muon L4/13	DAQ Ship to CERN	9/04	9/04	12/04	3
Trig/DAQ						

13. NSF COST SCHEDULE STATUS REPORT

Fourteen US ATLAS institutions will receive funding under the NSF Cooperative Agreement (No. PHY 9722537) in FY01. Technical progress reports are given in the respective subsystem paragraphs of Section 4. The NSF Cost Schedule Status Report (CSSR) in this section covers these 14 institutions, in addition to the Education, Institutional Dues and Common Project items which will be funded by the NSF, and also the Items Outside Approved Baseline and Contingency.

Status through the month of July 2001 reflects the new baseline schedules for all subsystems. The schedules are resource-loaded to the baseline funding of $163,750K with Contingency, Management Contingency and Items Outside of the Approved Baseline shown on separate lines, excluding all NSF R&D funds. The anticipated NSF contribution to the baseline funding is $60,800K

We note that more than half of the universities in the NSF CSSR are, or have been, funded by both NSF and DOE, while we manage the project without distinguishing the agency source of funding. For this reason, the NSF+DOE Budgeted AY$s column in Table 13-1 includes all Project funds allocated to each institution, while the last two columns to the far right show the contribution of each agency.

The re-baseline date was established as October 1 2000 and the FY 01 Estimate to Complete (ETC-01) was defined as all tasks and resources required too complete the project. These tasks were scheduled and the necessary resources were loaded into the schedules. All prior efforts were equated to the actual cost expended. There was a negative schedule variance along with a positive cost variance in the old baseline and this resulted in a reduction in both the work scheduled and the work performed in the new baseline.

The CSSR shows that $23,840.2K of the work has been completed which represents approximately 41.9% of the work authorized to date. There is an unfavorable schedule variance of $338.8 or 1.4% behind the plan and a favorable cost variance of $94.6K or 0.4% under spent for the work accomplished. There are outstanding commitments of $888.1k at this time that do not show up in the performance.

Schedule Variance

Hampton – SV = ($109.9k)

WBS 1.2.1.1.3 Barrel Module Component Assembly is behind plan $109.9k

Cost Variance

Although the overall cost variance for NSF Institutions is a favorable $154.6k it is comprised of both positive and negative variances as follows:

- Brandeis – CV = ($164.9k)
  - Over spent on tooling ($58.3k)

  - Charging against Global System Production tasks ($106.6k)
- Harvard – CV = ($154.6k)
  - Over spent on Common Procurements ($90.1k)
  - Chamber Construction ($52.0k)

- Nevis – CV = ($76.0K)
  - Over spent on the FEB ($155.3k)
  - Offset by small positive CV in the ROD System and Beam Tests

- MSU CV = ($93.5K)
  - Over spent on Extended Barrel Optics ($30.6k)
  - Over spent on Trigger/DAQ ($62.8k)

- University of Rochester CV = $549.2K
  - Under spent by $343.7k on Vendor Manufacturing but shows an outstanding commitment of $317.8k
  - Under spent by $163.9k on Manufacturing Monitoring

- University of Texas Arlington CV = ($121.5K)
  - Over spent by ($50.9k) on the Intermediate Tile Calorimeter Production
  - Reported $60k of prior year cost

- University of Chicago CV = $231.3K
  - Under spent by $253.1k on Readout
  - Over spent by ($35.2k) Extended Barrel Module

Table 13

Cost Schedule Status Report

Reporting Period Ending:7/31/01

	Cumulative To Date (k$)					At Completion (k$)			Complete (%)				
	Budgeted Cost		Actual Cost	Variance		NSF + DOE	Latest					Budgeted AY $s	
	Work	Work	Of Work			Budgeted	Revised					NSF	DOE
Institution	Scheduled	Performed	Performed	Schedule	Cost	AY $s	Estimate	Variance	Scheduled	Performed	Actual		
Brandeis	1,832.0	1,823.7	1,988.6	(8.3)	(164.9)	2,848.5	2,848.5	-	64.3	64.0	69.8	2,413.3	435.2
Harvard	2,818.1	2,809.4	2,964.0	(8.7)	(154.6)	6,909.4	6,909.4	-	40.8	40.7	42.9	6,909.4	
Columbia Nevis Lab [2]	3,516.6	3,512.4	3,648.4	(4.2)	(136.0)	9,458.1	9,458.1	-	37.2	37.1	38.6	9,196.8	261.3
Hampton University	1,015.1	905.2	899.3	(109.9)	5.9	1,495.3	1,495.3	-	67.9	60.5	60.1	1,495.3	
Michigan State University	598.2	570.8	664.3	(27.4)	(93.5)	1,075.5	1,075.5	-	55.6	53.1	61.8	1,040.2	35.3
Oklahoma	132.5	132.5	139.5	-	(7.0)	393.7	393.7	-	33.7	33.7	35.4	342.3	51.4
Pittsburg	519.0	519.0	550.8	-	(31.8)	2,033.6	2,033.6	-	25.5	25.5	27.1	1,920.1	113.5
SUNY Stony Brook	484.9	478.6	505.0	(6.3)	(26.4)	1,089.1	1,089.1	-	44.5	43.9	46.4	1,083.9	5.2
University of California Irvine	644.5	591.6	591.0	(52.9)	0.6	2,010.4	2,010.4	-	32.1	29.4	29.4	1,715.8	294.6
University of California Santa Cruz	3,318.0	3,306.5	3,251.6	(11.5)	54.9	3,984.5	3,984.5	-	83.3	83.0	81.6	3,286.3	698.2
University of Rochester	5,039.1	4,986.2	4,437.0	(52.9)	549.2	9,287.6	9,287.6	-	54.3	53.7	47.8	8,936.7	350.9
University of Texas Arlington	928.3	909.0	1,030.5	(19.3)	(121.5)	1,534.7	1,534.7	-	60.5	59.2	67.1	1,431.0	103.7
University of Chicago	2,049.8	2,047.8	1,816.5	(2.0)	231.3	2,126.9	2,126.9	-	96.4	96.3	85.4	2,115.4	11.5
Washington	1,282.9	1,247.5	1,259.2	(35.4)	(11.7)	3,241.0	3,241.0	-	39.6	38.5	38.9	3,241.0	
Education [3]				-	-	286.5	286.5	-	-	-	-	286.5	
Institutional Dues [3]				-	-	2,036.6	2,036.6	-	-	-	-	1,930.4	106.2
Common Projects [3]				-	-	7,142.5	7,142.5	-	-	-	-	652.2	6,490.3
Sub Total	24,179.0	23,840.2	23,745.6	(338.8)	94.6	56,953.9	56,953.9	-	42.5	41.9	41.7	47,996.6	
								-				-	
Items outside baseline						2,388.5	2,388.5	-				2,388.5	
Management Contingency						4,921.7	4,921.7	-				4,921.7	
Contingency						4,219.9	4,219.9	-				4,219.9	
Project Management						1,273.3	1,273.3	-				1,273.3	
							-						
Total (with DOE Funds included)	24,179.0	23,840.2	23,745.6	(338.8)	94.6	69,757.3	69,757.3	-	34.7	34.2	34.0		8,957.3
Total NSF Funds												60,800.0	
												60,800.0	69,757.30
												-	

Note
1. Not used
2. Nevis Costs do not currently include Project management costs
3. Treated as LOE based on actuals reported

14. DETAILED TECHNICAL PROGRESS

1.1 SILICON

Milestones with changed forecast dates:

1.1.1.1.1 Design

Milestone	Baseline	Previous	Forecast	Status
Support tube CDR	20-Jun-01	11-Jul-01	16-Oct-01	Delayed (See #1)
Cables/services CDR	20-Jun-01	11-Jul-01	10-Dec-01	Delayed (See #2)
Release bid for Support tube	4-Dec-01	4-Dec-01	5-Oct-02	Delayed (See #3)
Support tube FDR	10-Dec-01	10-Dec-01	26-Feb-02	Delayed (See #4)
Release bids for support	18-Dec-01	18-Dec-01	5-Oct-02	Delayed (See #5)

Note #1, 3-5 Design scope increased to support beam pipe, many interfaces to be resolved with other systems.
Note #2 Gap decision requires some redesign..

1.1.1.1.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
Complete disk development	16-Oct-01	16-Oct-01	15-Jul-01	Completed
Support tube development complete	10-Dec-01	10-Dec-01	26-Feb-02	Delayed (See #1)

Note #1 Design scope increased to support beam pipe, many interfaces to be resolved with other systems.

1.1.1.3.1 Design

Milestone	Baseline	Previous	Forecast	Status
FE-I1 spec complete	16-May-01	16-Jul-01	1-Sep-01	Delayed (See #1)

Note #1 Specification has been started, and was supposed to be ready for June review. Testing of Analog Test chip has taken priority.

1.1.2.1.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
Test Systems Complete	3-Aug-01	3-Aug-01	3-Oct-01	Delayed (See #1)

Note #1 The wafer test systems are operational and qualified for production. Some work is continuing to reduce test time and add some improved tests. It is expected that this will be complete by October when the large volume of production wafers starts to arrive.

1.1.2.1.3 Production

Milestone	Baseline	Previous	Forecast	Status

Complete preproduction fab	28-Feb-01	30-Jul-01	10-Aug-01	Delayed (See #1)

Note #1 The last of the 5 pre-production lots was delivered with one out of spec fab parameter. We gave Atmel a conditional waiver in that we said we would first test the wafers and then determine to accept them only if the out of spec parameter did not effect yield or performance. Atmel has also delivered some extra wafers to augment the last lots which did yield poorly. We have not tested all the wafers and therefore have not accepted the last lot. The remaining wafers should be tested by mid-August so that we can complete acceptance.

1.1.1 Pixels — Murdock Gilchriese (Lawrence Berkeley Lab.)

1.1.1.1 Mechanics

A "pixel mechanics week" was held at CERN in mid-July. There were two days of reviews by TC, including a successful PRR for the disk sectors and barrel staves. There have been some design modifications since the US pixel baseline was established. In the current design, the entire pixel detector and ID-region beam pipe are integrated on the surface, lowered as a package and inserted into the pixel support tube. The B-layer is no longer installed in the pit. This eliminates the B-layer support shell (a US deliverable), simplifies the B-layer support and services design and reduces material. This is the current design direction of the pixel group, in accord with TC, but assumes the development of the double-walled beam pipe (allowing bakeout with the B-layer in place) will be successful. This will only be known for sure by early 2002, so there is some risk in the current approach. A draft integrated European-US mechanics schedule was created for the TC reviews, and will be updated over the next few months. The schedule work is being done in the US. The design of the pixel support tube (PST) is proceeding but there are many interfaces to the SCT and beampipe to define. In addition, radioactivation in the forward region is not yet well quantified and may have a dramatic impact on the design of the endplug (PP1) region. Thus the design of the PST and related items will inevitably be slower than our baseline estimate, and costs are likely to increase as a result.

1.1.1.2 Sensors

Pre-production wafers from Tesla still have not been delivered. The qualification of a standard double-side chuck for wafer probing is going more slowly than planned. Nevertheless there remains very substantial slack in the schedule.

1.1.1.3 Electronics

Progress on the layout and verification of the front end IC remains steady and a submission in September remains the goal. Recent IBM turn-around times have been as low as five weeks, so it is possible that wafers will be delivered in November, roughly on the baseline schedule. Similar work on the MCC chip in Genoa is proceeding on the same schedule. The engineering effort on the comprehensive test system has been increased. The increased effort should just make it possible to complete the test system in time to be used with the IBM chips. There may be some cost increases as a result of the increased engineering.

The need for additional vendor-supplied test equipment has recently been identified and will be included in the ETC02 estimates.

1.1.1.4 Hybrids

The layout of the flex hybrid (v 3.x) compatible with the IBM FE chip and the existing AMS MCC was completed. The layout of the hybrid 4.x that is compatible with the IBM MCC is 90% the same as the v 3.x.

1.1.1.5 Modules

We continue to have problems making 8" dummy wafers that will be used to develop the bump bonding processes. The vendor believes it can correct the latest problem and has promised to make additional wafers at no cost to compensate for the delay.

Thermal cycling tests of existing dummy modules mounted on disk sectors are continuing at a cautious pace. The failure of the first solder-bumped module is not understood, although it may be that this module was simply badly made (one chip fell off during handling, X-rays indicated undersized bumps). Cycling of an indium-bumped dummy so far shows no failure, but a very substantial program of work remains in this area once more dummy modules are available. Given the IC schedule there is ample time for these studies.

Wafer thinning has started with another vendor and first results are encouraging. A thickness of 125 microns was achieved and the wafers undergo a stress-relieving process that makes them much easier to handle (more like paper and less like potato chips).

1.1.1.1 Mechanics

1.1.1.1.1 Design

Milestone	Baseline	Previous	Forecast	Status
Cables/services CDR	20-Jun-01	11-Jul-01	10-Dec-01	Delayed (See #1)
Disk Sector PRR	20-Jun-01	--	12-Jul-01	Completed
Global Support CDR	20-Jun-01	--	11-Jul-01	Completed
Support tube CDR	20-Jun-01	11-Jul-01	16-Oct-01	Delayed (See #2)
Global Support FDR	16-Oct-01	--	16-Oct-01	On Schedule
Release bid for Support tube	4-Dec-01	4-Dec-01	5-Oct-02	Delayed (See #3)
Support tube FDR	10-Dec-01	10-Dec-01	26-Feb-02	Delayed (See #4)
Release bids for support	18-Dec-01	18-Dec-01	5-Oct-02	Delayed (See #5)

Note #1 Gap decision requires some redesign.

Note #2-5 Design scope increased to support beam pipe, many interfaces to be resolved with other systems.

Eric Anderssen (Lawrence Berkeley Lab.)

Sector Production Drawings and Tooling design

All drawings for parts and subassemblies of the sector have been issued and are ready for approval. Both LBNL and ATLAS Drawing/Document control numbers have been assigned and placed on the drawings and the final versions uploaded into the appropriate nodes of the ATLAS EMDS database. The approval cycle has not been initiated in EDMS as the approval cycle has not been defined for the mechanics nodes in EDMS. Essentially this only requires defining a list of approvers, as the cycle and methodology are already defined. This should happen by end of August.

CAD models exist for all fixturing and tools for Sector production, drawings for the In-Plane bend of the sector tubing have been issued to the LBNL shop for fabrication. Remaining parts need to be detailed, and drawings issued.

Preliminary CAD models are complete for the Sector Thermal QA fixture. Modifications for manufacturability are underway. Detailed drawings to be issued for fabrication in August. The Student working on this project will continue, half time, through the semester for continuity.

Pixel Support Tube (PST)

An engineering note documenting current FEA results for a wide range of the parameter space already performed is being prepared. This will both support and focus decisions for directions of future analysis on the tube design. The support conditions and support designs themselves were heavily discussed at an Inner Detector Engineering meeting held at CERN after the CDR. There are some conflicting issues to resolve before proceeding, primarily concerned with the supports at the forward ends of the PST. There is concern over potential induced loads in the ID Barrel at the mounts to the SCT Barrel. Several options to reduce the magnitude of this load were put forth including decreasing the stiffness of the forward PST, or removal of the support entirely and increasing the stiffness of the forward PST. The aforementioned Engineering Note will guide which direction to proceed.

The design of Flexures for use in the supports was questioned by some reviewers as being too stiff in the soft direction. This is a function of the specific design chosen for the flexures in question and will be looked at in more detail to understand if an intermediate solution meets specification. (Requested reduction in stiffness also reduces stiffness in undesirable directions).

Responsible parties in TC have been identified to address questions about space constraints during installation. Discussions of Survey and Alignment were inconclusive, but indications are that radial adjustability of Beam Vacuum and PST relative to beam center are not necessary. TC needs to lay out what is and isn't required and how much is necessary.

Design work for the Pixel mounts (Global Support to PST interface) has begun. Goals set include a prototype mount to be integrated into the PST Mockup, mounted on a frame model.

Murdock Gilchriese (Lawrence Berkeley Lab.)

General

A Conceptual Design Review of most of the pixel mechanics (services and the pixel support tube were presented at a pre-conceptual level) was completed successfully at CERN. The PRR for the Disk Sectors (and Barrel Staves) was also completed successfully. In addition to the two days of review, the remainder of the week was spent in specialized meetings on the pixel mechanics and related interfaces. Four important points arose during these meetings. First, it was decided to focus all design effort on a pixel installation scenario in which all elements of the pixel detector + the beam pipe are integrated on the surface and lowered as a package into the pit. In the previous design concept the B-layer was installed in the pit and its services therefore exited from one end of the detector, passing at low radius through one of the disk sections. In the new design, the B-layer services follow the same routing as the other barrel layers, thereby reducing the material in the active region. In addition, the B-layer support shell (a US deliverable) is eliminated. Second, the importance of activation of the beam pipe within the ID and of the pixel elements, particularly the patch panel PP1 located at the end of the ID was discussed with Nessi and TC. It is not yet clear if it will be possible to stand at the end of the ID and disconnect services and pipes from PP1. This was flagged as an urgent item to be address by TC and the pixel team by September-October. The design and fabrication of PP1 is a US deliverable, but most of the design will be delayed until the activation issue is resolved. Third, the pixel support tube (PST) has many interfaces with the SCT and now the beam pipe. Resolving these interfaces will introduce delay not foreseen in the baseline schedule. Fourth, an integrated schedule for US-Europe mechanics deliverables was created for the design reviews. This was largely done in the US. The integrated schedule disagrees in some respects from the current US baseline schedule. The integrated mechanics schedule will continue to evolve over the next few months before a new overall ATLAS pixel schedule is baselined. There is excellent communication between the US and Europe on the new schedule, which will form the basis for the ETC02 baseline by the end of the year.

Disk Sectors

The design of the disk sectors, apart from coolant fittings, is complete. However, the drawing set has not gone through the formal approval cycle but is expected to do so in August. We do not as yet have a final solution for the coolant fittings. There are two variants still under active consideration (see Prototypes/Development).

Disk Rings

The design of the disk rings is complete. Production tooling drawings and a full set of drawings for an RFQ were nearing completion at the end of July.

Support Frame

The conceptual design of the support frame and end cones is complete. The next step is to compare FEA estimates of the end cone properties with the measurements of the prototype. And the interface between the frame and the supports to the pixel support tube must be detailed.

Sally Seidel (University Of New Mexico)

On the PP2/cable project, the current layout of the connectors for the Type II cables uses one connector per cable (50 connectors total) and the result is that the connectors just barely fit on the 150mm x 450mm PP2 side panel. The concern is that the connectors may be too close together and one may not be able to mate/demate them because the connector shells are practically touching each other. Drawings were generated to build a prototype panel. We are waiting for the delivery of the connectors, which have a 6-week lead-time. Alternate connectors (multipin LEMO) were selected and ordered to continue the prototyping effort.

1.1.1.1.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
Complete sector development	20-Jun-01	--	15-Jul-01	Completed
Complete disk development	16-Oct-01	16-Oct-01	15-Jul-01	Completed
Complete global support development/prototypes	16-Oct-01	--	16-Oct-01	On Schedule
Complete B-layer shell prototype	10-Dec-01	--	10-Dec-01	See Note #1
Support tube development complete	10-Dec-01	10-Dec-01	26-Feb-02	Delayed (See #2)

Note #1 The design of the B-layer support has been changed to eliminate this item.

Note #2 Design scope increased to support beam pipe, many interfaces to be resolved with other systems.

Neal Hartman (Lawrence Berkeley Lab.)

INSTALLATION MOCKUP

Drawings for the material friction tester have been completed and submitted for fabrication. Two samples of 1/2" VESPEL rod (polyimide) arrived from the manufacturer; one is filled with teflon, while the other is filled with molybdemum disulfide. A 1/2" thick plate of Ryton PPS (polyphenylsulfide) arrived, which is potentially the lowest friction material available. However, contrary to previous thought, the sample appears to be filled with carbon, and is flaky and dusty to the touch. This probably precludes its use as a detector sliding contact, but it will be machined into a test piece and measured with the friction tester nonetheless.

COOLING SERVICES

Tubes and fittings were sent to a local vendor for laser welding. Based on past success, this has been determined the baseline joining method (unless electrical isolation concerns demand the use of plastic fittings - most likely PEEK). Laser welding development now centers on finding a local vendor that can meet fabrication quality requirements.

Aluminum/PEEK Luer lock fittings have been fabricated, leak tested, and proof tested to 150 psig. Results on 7 of 8 fittings are good, with leak performance in the low 9 and 10 scale (He). The remaining fitting does not seal for unknown reasons.

Neat resin samples have been made for irradiation testing in C_3F_8, in order to further investigate the "oozing" behavior observed in previous tests. Samples with a silane adhesion promoter have been created, but samples without the silane have yet to be made (it is believed that silane may be one of the causes of the observed oozing action, since it was the only variable in the single test where oozing was noticed). In addition, new, un-irradiated C_3F_8 will be used, since oozing was only observed in a test that used highly irradiated C_3F_8. All samples will be irradiated to 25 MRad.

At the CDR/PRR meeting in CERN during the month, the fitting specifications and testing regimen were discussed and modified. The new testing regimen is as follows:

1.) He vacuum leak check (quantitative)

2.) 10 bar proof test (visual, assure that fitting doesn't mechanically explode, no more than 1 minute)

3.) 4 bar He pressurized leak check at 0 Celsius (quantitative)

4.) 1 bar He pressurized leak check at -35 Celsius (quantitative)

5.) He vacuum leak check (quantitative)

6.) Thermally cycle fitting assembly 50 times (20 to -35 C)

8.) Pressure cycle fitting assembly 50 times (1 to 4 bar)

9.) Repeat tests 1,3,4,5 (all quantitative, in that order)

All pressures are given as absolute. Each potential seal type must have at least 10 specimens to run through the above sequence. If plastic seals are considered (as at LBNL) then an additional 10 fittings must undergo the same tests after irradiation to 25 MRad, in order to compare with the control group.

The fitting specifications were also changed as follows:

1.) Permanent connections (welds, etc.) vacuum leak check to 10^{-7} atm-cc/sec He.

2.) Seal leak rates under vacuum are $3x10^{-5}$ atm-cc/sec He.

3.) Seal leak rates at 4 bar are 10^{-4} atm-cc/sec He.

In order to determine if the system conductance is high enough to pump down to initial vacuum (before introducing C_3F_8), a rough estimate of the conductance and pressure for given fitting leak rates was calculated. It was assumed that there are 10 fittings per cooling circuit, equal leak rates for all fittings, and a lumped global system conductance (meaning that all pipes and sizes are considered, but they are all lumped into one series conductance or resistance). This may be an optimistic estimate, but it shows that for the proposed seal leak rate ($3x10^{-5}$), the system will arrive at a minimum pressure (in the capillary) of more than 175 microbar. It is unclear that this pressure is acceptable, so leak rates may need to be manipulated in the future.

Murdock Gilchriese (Lawrence Berkeley Lab.)

Disk Sectors

Evaluation of prototype disk sectors is complete. Thermal qualification of recent prototypes was documented in an ATLAS note.

Disk Rings

Placement of the prototype disk ring in the prototype end frame was completed. The ring was removed, reinserted and measured. The repeatability of placement appears to be better than 0.001". The procedure for drilling holes in the frame, inserting bushings and placing the ring works well.

Support Frame

The fabrication of a prototype end cone was completed and testing began.

1.1.1.1.3 Production — Murdock Gilchriese (Lawrence Berkeley Lab.)

Validation tests on the carbon-carbon plates for disk sectors and rings continued. Tensile and thermal properties were found to be within specification. The initial attempt by the vendor to resin impregnate the material was not acceptable and their method modified. Their last samples were acceptable and the vendor has been given the go ahead to cut the material for production.

Bending tests on annealed tubes for the disk sectors have given good results. Bonding tests of two types of PEEK to carbon-carbon are under way (the PEEK is used in the sector construction). About one-half of the production tooling drawings have been submitted to the shops for fabrication. The remainder of the detailed drawings are still to be completed in August.

1.1.1.2 Sensors

1.1.1.2.1 Design

Milestone	Baseline	Previous	Forecast	Status
Compl. Spec for production order release	12-Mar-01	--	15-Sep-01	See Note #1
ATLAS PM approval of production procurement	23-Jul-01	--	1-Oct-01	See Note #2
Release initial MC for sensors/testing	23-Jul-01	--	1-Oct-01	See Note #3

Note #1-3 Production is planned to begin in January 2002. Since there is considerable slack in the sensor schedule, this has no impact on the global schedule.

1.1.1.2.2 Development/Prototypes — Sally Seidel (University Of New Mexico)

Acceptance testing of preproduction wafers has continued. This process is being used to refine procedures as well as qualify wafers so consequently requires more time than will be necessary during production. IV measurements (QA procedure 6) have been completed on the tiles and single chip structures. CV measurements have been performed on tiles (3 per wafer), single chip structures (6 per wafer) and mini chips (2 per wafer) on wafers 4455-11, 4457-07, 4457-12, 4458-03, 4458-14, and 4458-08. New Mexico has posted results of the measurements on the preproduction cross-calibration wafer at http://www-hep.phys.unm.edu/atlas_pixel/xcalibration3/. All of the probing institutes are encountering significant challenges in adapting the Dortmund backside probing fixture for use outside Dortmund. Mechanical problems adapting it to the UNM probe station mean we will have to either purchase a stage to provide z-axis adjustment or use it with a different microscope. We are currently in the process of assembling the UNM backside probing chuck. This only affects QA Measurement Procedure #10 (IVgate on MOSFET).

1.1.1.3 Electronics

1.1.1.3.1 Design

Milestone	Baseline	Previous	Forecast	Status
FE-I1 spec complete	16-May-01	16-Jul-01	1-Sep-01	Delayed (See #1)

Note #1 Specification has been started, and was supposed to be ready for June review. Testing of Analog Test chip has taken priority.

Kevin Einsweiler (Lawrence Berkeley Lab.)

We continue to place all of our design resources on the deep-submicron design effort. We have worked to characterize the IBM version of our test chip. Due to shipping delays, we only received these chips at the beginning of July, more than one month after the expected arrival date. Since we have failed to extract reliable estimates of the critical capacitances (injection and feedback) from lab measurements, we have chosen to use the extracted values of the capacitances (calculated from the layout using typical process parameters). This procedure should have about a +/-20% uncertainty, so none of the numbers below involving electrons should be believed to better than this uncertainty.

Most aspects of the IBM chip seem to perform identically to the TSMC chip. There are two exceptions. First, the threshold dispersion for the IBM chip appears to be much lower than for the TSMC chip. We expected it to be slightly lower (simulations predicted about 1800e sigma instead of the 2400e observed for TSMC). We observe a dispersion of only about 1200e sigma. Second, the timewalk performance of the IBM chip is significantly worse than that of the TSMC chip. For TSMC, the performance was acceptable, although worse than simulation. With the expected detector load of 400fF, we need 2000e above threshold to produce an output which is delayed by no more than 20ns compared to the large charge limit. For IBM, the required overdrive is about 2.5 times worse, which is unacceptably poor. This appears to be due to poor risetime in the second stage of the front-end in the IBM chip. Simulations indicate that the risetime of the second stage in IBM and TSMC should be almost identical, with IBM being slightly better, and should be in the range of 20-25ns depending on the charge value. Since the layout was "identical" for TSMC and IBM, this is very difficult to understand, and we are presently investigating further.

Meanwhile, work is continuing on all aspects of the complete FE-I chip. The front-end used in the IBM test chip has been implemented in the full FE-I chip. All of the supporting blocks for the chip have been integrated into the bottom of column region. This includes a total of 13 DACs and 156 control bits, all of the biassing generation, and all of the bussing needed to distribute the control and digital signals to the entire matrix. The layout and interconnection for the digital blocks in the pixel, bottom of column, and end of column have been fully integrated, and are undergoing verification using Verilog for functional simulation and TimeMill for timing simulation. The complete digital part of the chip should be completed within 2 weeks. For the analog parts of the chip, there are still some minor layout updates, based on the measurements of the test chips. These include small adjustments of capacitor sizes, and scaling of bias currents, plus a good scheme for external charge injection to cross-check the present internal injection scheme. We have performed a first DRC on the layout, and there are a rather small number of errors. The schematics are nearing completion also, so it should be possible to do a complete LVS starting in about 2 weeks. We expect to have completed the entire chip by mid-September, pending a better understanding of some of the test chip measurements, and pending further top-level timing and functional simulations, leading to a submission towards the end of September.

As the pinout of the FE-I has become frozen, we are beginning to work on the necessary probe cards and support cards required for testing wafers, single die, and modules. All of these cards need to be updated, because of major changes to the pinout required to meet the production module mechanical envelopes. These cards will all be modified and re-fabricated over the next few months, in order to have everything ready in time for the returning wafers, now estimated to be about the end of November (assumes 8 week turnaround, including resolving last minor DRC errors, since IBM requires individual waivers for all residual DRC errors).

In order to exercise the next generation of chips from ATMEL and IBM to the fullest extent possible, and in particular to develop the capability to label chips as "known good die", and be sure that this classification will remain true after exposure to the full radiation doses of ATLAS, we are developing an improved test system.

We have continued testing of the first PLL boards received. This work has received reduced priority because of the many other constraints on our time. The power and clock distribution are working, including the new programmable frequency clock generator which does work up to the required 100MHz, and the VME interface is working. The basic data paths and memories in the module have also been tested, and so far the only errors found have been VHDL errors. This effort should soon receive additional manpower from the ROD effort once the ROD pre-production boards are submitted for fabrication, and we intend to give the debugging high priority during early September, in order to complete the module on that timescale. Prior to mass-production of the cards for the collaboration, we need to revise the PC board to include additional logic needed for decoding 80Mbit/s data streams (this capability was missing from the first version - it was simply forgotten in the rush to get the board done). However, the first three PC boards that we have fabricated will be adequate for initial testing of FE-I wafers.

We have now completed the PICT schematics and they were reviewed in mid-July. A list of actions was produced as a result of the review, and all of the required modifications suggested by the reviewers have now been implemented in the schematics. The package geometries for all parts have been entered into Mentor. The layout of the board will start seriously in about 1-2 weeks when the ROD pre-production prototype board is completed. We expect to be able to submit this board for fabrication no later than the end of September.

The accumulated delays in the PLL and PICT effort due to the relatively low quality of engineering manpower available now show some signs of improvement. There will be an additional engineer part-time on the PLL starting in a few weeks, and there will be an additional engineer part-time on the PICT starting immediately. Both are senior engineers with extensive experience in these types of boards. We hope that with the injection of this additional manpower, we can complete and debug a limited number (perhaps 3) of the boards by end of October. This should allow us to cope with the initial wafer testing of the FE-I chips. However, it is clear that we will be very late in delivering these new test systems to the collaboration at large, and this will cause additional frustration and some modest delays in the project schedule.

K K Gan (Ohio State)

The VDC-D2/DORIC-D2 on the irradiated opto-board has been studied. One link has a broken fiber and hence we do not know the status of the link after the irradiation. For two of the links, the PIN current threshold for no bit error increases from 15 and 60 uA to 24 and > 120 uA. For the other link, the threshold increases from 17 uA to over 170 uA but the low threshold can be restored by increasing the supply voltage slightly, from 3.2 to 3.35 V. Based on these results and the results on the irradiated VDC/DORIC in the cold box, the radiation hardness of DMILL is deemed inadequate for the Pixel detector.

We have received the IBM version of optical dice, VDC-I1 and DORIC-I1. There are two versions of VDC: one is the IBM version of the DMILL die and the other decouples the adjustment of the bright and dim currents. The dim current in the former version is observed to rise to 4 mA with 40 mA bright current while the dim current in the latter version remains constant at ~1 mA as designed. The dice have fast rise and fall time, <1 ns. The dice of the latter version also have a large overshot, a consequence of the fast rise time. They also consume large current, ~30 mA for ~20 mA of VCSEL bright current, higher than the DMILL dice.

The DORIC-I1 dice are more problematic. The d-control circuit oscillates but can be cured with an external 1.2 nF capacitor. We observe an offset at the two differential inputs of the pre-amp. This is verified with the adjustable DC feedback designed to cancel the offset. The feedback circuit can only cancel a small offset as expected (The RC time constant in DORIC-D3 submitted to DMILL after the IBM submission was greatly increased in order to cancel a larger offset.)

For the next IBM submission, there will be two versions of VDC-I2, single- and four-channel versions. The tentative decision is to implement the VDC design that decouples the adjustment of bright and dim currents. The dummy circuit that turns on while the VCSEL is off (dim) to maintain constant current consumption will be improved to consume several mA less current. For DORIC-I2, the following improvements are planned:

1. larger time constant in d-control to stop oscillation: increase the capacitance from 200 fF to 1 pF.

2. larger time constant in pre-amp with new duty cycle control loop to reduce clock jitter with random data. This has already been implemented in the DMILL submission.

3. add a bias circuit with the voltage fixed by a resistive potential divider which simulates well at all corner transistor parameters, unlike the bias circuit in the current dice which is predicted to fail at some corner parameters.

1.1.1.3.2 Development/Prototypes

Milestone	**Baseline**	**Previous**	**Forecast**	**Status**
FE-D3 submitted	2-May-01	--	2-Dec-01	Delayed (See #1)
1st IBM prototype submitted (FE-I1)	26-Jul-01	--	17-Sep-01	Delayed (See #2)
FE-D3 wafers arrive	22-Aug-01	--	22-Aug-01	Delayed (See #3)
1st IBM prototype delivered	24-Oct-01	--	12-Nov-01	Delayed (See #4)
Complete initial wafer probe FE-I1	7-Nov-01	--	26-Nov-01	Delayed (See #5)

Note #1, 3 We have delayed all further work on FE-D3 pending submission of FE-I1 and study of its performance. At the present time, no further DMILL submissions are foreseen unless significant problems are observed with 0.25u designs

Note #2, 5 Testing of the Analog Test chip has revealed large threshold dispersion. This must be improved before full submission. Other accumulated delays suggest a total two-month delay in the submission date.

Note #4 See note #2 above. Note that due to reduced foundry demand, the turnaround for IBM has been observed to be as low as 5 weeks, so the 8-week processing time assumed here should be reasonable.

1.1.1.4 Flex Hybrids/Optical Hybrids

1.1.1.4.1 Design

Rusty Boyd (University of Oklahoma)

Flex Hybrid Design (UOK)

The design and layout of the flex hybrid v3 was completed in late July. The design files have been made available to the Pixel collaboration for review and comment. Flex hybrid v4 is thus about 90% complete. Work will continue on v4 after v3 has been submitted for fabrication.

1.1.1.4.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
Initial Flex 3.x tests complete	13-Dec-01	--	13-Dec-01	On Schedule

K K Gan (Ohio State)

We have prepared an opto-board for the September irradiation. The first prototype opto-board is used instead of the second prototype opto-board because the former allows dice to be placed in close proximity to the opto-packs to achieve low PIN current threshold. We are currently awaiting the delivery of the Taiwan opto-packs for mounting.

Rusty Boyd (University of Oklahoma)

Flex Hybrid Development (UOK)

We have received the high voltage capacitors irradiated at CERN PS during May of this year. These were irradiated under 700 Vdc and will be tested both with and without voltage applied. We are currently upgrading our data acquisition and analysis software for these tests.

We have also been assembling v2 flex hybrids and the pigtail and LBL mini support card for these flex. This allows us to begin test development for assembled flex circuits. The first step is to implement a relay multiplexer in combination with test instruments and the pigtail and support card. Much of this is software development in the Labview environment. This should allow rapid, first order assessment of the quality of the flex hybrid by insuring that there are no shorts or opens in the power and module I/O connections.

1.1.1.4.3 Production

Milestone	Baseline	Previous	Forecast	Status
Start initial production buy of components	13-Dec-01	--	13-Dec-01	On Schedule

1.1.1.5 Modules — Maurice Garcia-Sciveres (Lawrence Berkeley Lab.)

LBL Module Assembly Status Report for July 31, 2001

Dummy Modules

A second module, this one Alenia, was mounted on a sector with CGL and thermal-cycled from room temperature to -35 deg. C 13 times with a 1-week storage period at room temperature after 3 cycles. No opens resulted in the monitored chains. The resistance of the monitored chains increased from 50K to 1M (4 column pairs in series) after room temperature storage. This was cleared with 100uA at 100V and the resistance dropped to 38K. Recall first thermal cycled dummy was IZM and it showed opens after overnight storage following 19 thermal cycles.

Hot Modules

A third flex V2 module using a CERN flex with MCC pre-loaded at Mipot and tested at Genova, and an IZM bare module is now fully wirebonded and ready to be tested. The second hot module (Alenia+compunetics) still does not operate. Suspect a bad MCC.

Dummy wafers

A 10-wafer run using oxide passivation that was due in July has failed due to over-etching. This was caused by operator error. A new run of 25 wafers has already been started with high priority and is expected August 10. There is no charge for this make-up run.

Wafer Thinning

A low melting point water-soluble wax has been successfully used to hold a blank 6" wafer during grinding to 100um thickness. Further tests to show that the wafer can be easily transferred to a second carrier wafer are on hold pending results from a new grinding vendor (Aptek). One bumped 6" wafer has been sent to Aptek for a test. This vendor specializes in thinning bumped wafers with a proprietary process (using wax to hold the wafers) followed by backside polishing to relieve stress. They can produce 100um thick 6" wafers that can be handled without being mounted on a carrier wafer. The wafers bend like a metal foil, but do not easily break. Special shipping boxes and handling tools for such wafers are available.

PP0

A service panel prototype is being constructed using G-10 instead of carbon fiber.

1.1.2 Silicon Strip System — Murdock Gilchriese (Lawrence Berkeley Lab.)

The SCT successfully completed the PRR for the front-end chip during the first week in July. This was followed by discussions with ATMEL to clarify the remaining issues needed to go into production. The first 520 wafers have been ordered and a release order to purchase an additional 155 raw wafers has been completed. An important goal for the chip production is to move to a different epi vendor as soon as possible based on a hoped for improvement in yield. Chips with the new epi layer have been tested at UCSC, diced, and shipped to Japan for the production of a few modules which will be used to verify that the chips made with the new epi layer produce radiation hard modules. These modules will be radiation tested soon. The wafer screening effort is continuing to make progress at UCSC. Problems with the tester stopping prematurely have been fixed through software improvements and testing is approaching a routine operation. Work, however, still remains to optimize (minimize) the test time and to finalize the set of test vectors, although we believe these improvements should be straightforward.

The hardware for module construction continues to make progress at LBNL. A major remaining issue is the production of baseboards and the scheme for precisely holding and aligning these. The completion of tooling requires a final solution to these issues. The baseboard preseries is due to arrive toward the end of the summer at which point final decisions can be made. If there are no problems encountered the entire set of baseboards are due to arrive by the end of this calendar year.

1.1.2.1 IC Electronics

1.1.2.1.1 Design

Milestone	Baseline	Previous	Forecast	Status
Production Readiness Review (PRR)	15-Jun-01	--	4-Jul-01	Completed

Alexander A. Grillo (University Of Calif. At Santa Cruz)

LBNL & UCSC

Most of the software resource issues have been resolved. Vitaliy Fadeyev from LBNL has taken over responsibility for the "online software" and Bill Murray from RAL the "offline software". Vitaliy will maintain the CVS repository for the software at LBNL. We still do not have any personnel to write the necessary database report programs to that we can obtain necessary and useful information from the SCT Database into which all the test data and material flow information is being stored.

A sticky problem with software control of the probe station at UCSC was finally solved. The problem appeared in June after a new release of the wafer test software was installed. It was later determined that the extension of this software to a multi-thread environment caused the communication links between the wafer test software and the prober control software to malfunction because the handshaking was no longer in sync. This was corrected by making the communication routines more multi-thread compatible. With this fix, we have been able to run successfully for the last half of the month with no prober control errors.

Work has started on the final test engineering work but it is not complete. This includes: some of the test vectors need to be combined for execution efficiency; the number of iterations of each test must be reduced in order to reduce test time while still maintaining acceptable reproducibility; and the new tests of the I/O timing and signal amplitudes must be added.

The June SCT Week showed that that the forward module program is in serious trouble. The new version of the hybrid appears to be very unstable electrically. Ned Spencer was asked to help with a new hybrid design to hopefully alleviate these problems. That is now taking up much of his time along with other systems engineering issues in the barrel and forward sectors.

1.1.2.1.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
Test Systems Complete	3-Aug-01	3-Aug-01	3-Oct-01	Delayed (See #1)

Note #1 The wafer test systems are operational and qualified for production. Some work is continuing to reduce test time and add some improved tests. It is expected that this will be complete by October when the large volume of production wafers starts to arrive.

Alexander A. Grillo (University Of Calif. At Santa Cruz)

LBNL & UCSC

The remaining pre-production wafers were tested this month at UCSC and at RAL. At month end, only 3 wafers remained to be tested at UCSC which will be completed the first week of August. There is still remaining work to be done with radiation testing in August. In particular, work to understand the large increase in digital current with some chips after full irradiation is on going.

1.1.2.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
Complete preproduction fab	28-Feb-01	30-Jul-01	10-Aug-01	Delayed (See #1)
Release/Start Full Electronics Production	6-Jul-01	--	15-Jul-01	Completed
First Lots Delivered	23-Nov-01	--	23-Nov-01	On Schedule

Note #1 The last of the 5 pre-production lots was delivered with one out of spec fab parameter. We gave Atmel a conditional waiver in that we said we would first test the wafers and then determine to accept them only if the out of spec parameter did not effect yield or performance. Atmel has also delivered some extra wafers to augment the last lots which did yield poorly. We have not tested all the wafers and therefore have not accepted the last lot. The remaining wafers should be tested by mid-August so that we can complete acceptance.

Alexander A. Grillo (University Of Calif. At Santa Cruz)

LBNL & UCSC

As hinted in the June progress report, the PRR for the ABCD was completed successfully on 4-July. Some recommendations were made by the review committee for additions to our QA plan. Those are now being implemented. Also, on 5-July, we met with ATMEL to discuss details of the production orders, delivery schedule and yield concerns. After several hours of discussion, our proposal was fully accepted that if the yield continues to fall below the minimum yield specified in the Frame Contract the wafer costs will be scaled down accordingly. This will maintain a ceiling cost for wafers at what we originally budgeted based upon the contract minimum yield. If higher yields are realized as ATMEL predicts based upon improvements in their line, our wafer costs will go down. We will experience higher test costs if the yield remains below the minimum projected yield of 26%.

The first batch of production wafers (only 35) will be shipped in mid-August. In October, we will start to receive regular shipments of 100 wafers every other week.

Plans are in place to qualify their new epitaxy sub-contractor in October so that we will start to receive wafers from that source before the end of the year.

1.1.2.2 Hybrids/Cables/Fanouts

1.1.2.2.1 Design

Milestone	Baseline	Previous	Forecast	Status
Hybrid Bid Evaluation Complete	11-Jun-01	--	15-Jul-01	Completed
ATLAS PM Approval of Maj Procs	20-Aug-01	--	20-Aug-01	On Schedule
Hybrid/Module Production Readiness Review	3-Sep-01	--	3-Sep-01	On Schedule
Complete Award Hybrid Contracts	14-Sep-01	--	14-Sep-01	On Schedule

1.1.2.2.2 Development & Prototype Fabrication

Carl Haber (Lawrence Berkeley Lab.)

Materials and documentation were organized in preparation for hybrid assembly and bonding tests to be done in August. A process for depositing the required uniform glue layer was tested and adopted. A bonding pull test process was specified and a results sheet composed. Work continued on dummy hybrid assemblies. A second version of the hybrid folding fixture was discussed and drawings begun.

1.1.2.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
1st Preproduction Hybrids Avail for Mod Assy	4-Jun-01	--	15-Sep-01	Delayed (See #1)
Compl Preproduction Assy	13-Aug-01	--	21-Oct-01	Delayed (See #2)
Compl Testing of Preprod Hybrid	3-Sep-01	--	21-Oct-01	Delayed (See #3)

Note #1 This will follow the hybrid design review and is set by Japanese procurement schedule. The FDR is complete but some minor mods have been circulated.

Note #2-3 Set by date of item1 above.

Carl Haber (Lawrence Berkeley Lab.)

1.1.2.3 Module Assembly and Test

1.1.2.3.1 Design of Assembly & Test Tooling

Milestone	Baseline	Previous	Forecast	Status

Compl Design of Preprod Mod Assy/Test	3-Sep-01	--	3-Sep-01	On Schedule
Module PRR	3-Sep-01	--	3-Sep-01	On Schedule

Carl Haber (Lawrence Berkeley Lab.)

Design work continues on the folding fixture version 2. After discussions with RAL, we are being sent revised drawings of the assembly window frame. We will join RAL in an order for new frames from Electro-Mec.

1.1.2.3.2 Development & Prototypes **Carl Haber (Lawrence Berkeley Lab.)**

The IV system software was completed. Documentation is in progress. Code was written to interface to the SCT database. The dark box has been ordered from the shop.

Work continued on improving the auto-focus system on the assembly platform. A new actuator was ordered for z motion control. We await new firmware to drive it from Newport.

Metrology was studied on the dummy modules. There is a sizable offset in X and the origin is being analyzed. Offsets in the mounting washers cone to hole alignment were studied as a possible source of this.

Work continues on dummy detectors in the UC microlab and with an outside vendor.

1.1.2.3.3 Production

Milestone	**Baseline**	**Previous**	**Forecast**	**Status**
Complete Preproduction Module Assembly	30-Jul-01	--	30-Oct-01	Delayed (See #1)
Complete Preproduction Module Testing	3-Sep-01	--	30-Oct-01	Delayed (See #2)

Note #1-2 Require pre-production hybrids which won't be available until the end of summer.

Carl Haber (Lawrence Berkeley Lab.)

IV scan code was interfaced to the SCT production database. Metrology analysis code was received from RAL and is being evaluated.

1.1.3 ROD Design & Fabrication **Dick Jared (Lawrence Berkeley Lab.)**

The VHDL code for the ROD has been written mostly tested and simulated. The CODE is now considered to be in maintenance mode. In the reporting period activity on VHDL has concentrated on simulating VHDL and testing operating code on the ROD. Code maintenance item have included EFB token data format and data order, upgrades to the program resources manager and controller front-end occupancy counters, trailer flag, bus bridge and serial links. DSP code has also been written to configure the front-end modules (not tested).

VHDL to test the wiring on the ROD has been written and is under test. This is special code that allows the test stand to test the integrity of the copper traces on the ROD. The code will be used in production.

The Rod is being upgraded to the production model. The Schematics have been upgraded to the production model. Layout of the PC is in progress and scheduled to be completed in August. Mechanical stiffeners have been added along with minor changes to the circuitry. Parts have also been ordered to complete inventory of parts need in the next few months. Production model cards are scheduled to be fabricated by September 25. These cards will be needed for user evaluation of the ROD.

1.1.3.4 ROD Test Stand

1.1.3.4.3 SCT/Pixel Test Stand Software

Milestone	Baseline	Previous	Forecast	Status
Production Diagnostic Test Stand Completed	29-Sep-00	--	29-Aug-01	Delayed (See #1)

Note #1 The test stand software is completely functional for the production testing. This software will be updated for more efficiency in the next few months. The remaining testing is of the hardware (fabricated) to loop back the outputs to the FIFOs at the input to the ROD. The loop back cards are used to verify the output data quality. These loop back cards will be tested when more RODs are fabricated.

1.1.3.6 ROD Prototype Evaluation

1.1.3.6.3 User Evaluation of ROD in Europe

Milestone	Baseline	Previous	Forecast	Status
SCT ATLAS Final Design Review	11-Jun-01	--	15-Nov-01	Delayed (See #1)
SCT ROD User Evaluation Complete	1-Oct-01	--	15-Apr-02	Delayed (See #2)

Note #1 The production model card are due to be fabricated and tested at LBL(3 ea.) by Oct. 10 2001. They will then be sent to Cambridge for testing to be completed by early November. The date for the review is predicated on the completion of the Cambridge test.

Note #2 The complete user evaluation is predicated as completion of the production model of the BOC and ROD. The prototype TIM will be used for the testing. The limiting factor is completion of the initial SCT DAQ. The SCT DAQ prototype is scheduled to be completed in October of 2001 and the usable DAQ will be ready in January of 2002. The DAQ and cards will be used at CERN in December 2001 to early April 2002 to verify that the SCT Off Detector Electronics function as expected.

1.1.3.7 ROD Production Model

1.1.3.7.1 Updating of ROD to production Model

Milestone	Baselin e	Previous	Forecast	Status

SCT ATLAS ROD PRR	1-Oct-01	--	15-Apr-02	Delayed (See #1)

Note #1 The PRR is contingent on completion of the user evaluation. Please see 1.1.3.6.3 SCT ROD user evaluation complete for details.

1.1.3.7.3 Evaluation of Production Model

Milestone	Baseline	Previous	Forecast	Status
Start Production Procurements	13-Apr-01	--	30-Jul-01	Completed
Release Production Dwg/Specs	16-May-01	--	15-Aug-01	Delayed (See #1)
Pixel ROD Design complete	14-Jun-01	--	15-Nov-01	Delayed (See #2)
Release Production Bids	4-Jul-01	--	20-Aug-01	Delayed (See #3)
Bid Evaluation Complete	15-Aug-01	--	7-Sep-01	Delayed (See #4)

Note #1 The current progress show that the drawing will not be ready till 15 August of 2001. This was caused by the extended time required to debug the proto ROD. Production is not expected to slip past the macro assembly site need date.

Note #2 The production model is scheduled to be tested at LBL and Cambridge by November 15, 2001.

Note #3 The first bid to be released is for the Production model and 5% production of PC cards (25 ea.). The large production bid will not be released till the user evaluation at CERN system test is complete. These cards are needed for the system test at CERN and evaluation of the ROD at the macro assembly sites.

Note #4 The delay will have no impact on needs.

1.1.3.8 ROD Fabrication

1.1.3.8.1 ROD 5% Production

Milestone	Baseline	Previous	Forecast	Status
Project Managers Approval 5% Production	1-Oct-01	--	18-Jul-01	Completed
Begin First End Cap SCT Module Ass/Test	25-Nov-01	--	25-Feb-02	Delayed (See #1)
Begin First Barrel SCT Module Ass/Test	27-Dec-01	--	27-Dec-01	Delayed (See #2)

Note #1-2 Projected by survey of the macro assembly sites.

1.2 TRT

Milestones with changed forecast dates:

1.2.1.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
HV Plates (Module #3) CUM #9 Available	30-Mar-01	30-Sep-01	30-Jul-01	Completed (See #1)
HV Plates (Module #2) CUM #12 Available	30-Mar-01	30-Jul-01	30-Aug-01	Delayed (See #2)
HV Plates (Module #2) CUM #14 Available	30-Apr-01	30-Jul-01	30-Aug-01	Delayed (See #3)
Module Assy #1 IU Module Assy CUM #7 Complete	30-Apr-01	30-Aug-01	30-Jul-01	Completed
Module Assy #2 Duke Module Assy CUM #9 Complete	31-May-01	31-Jul-01	31-Aug-01	Delayed (See #4)
Shells (Module #1) CUM #16 Available	31-May-01	31-Jul-01	31-Aug-01	Delayed (See #5)
Shells (Module #2) CUM #15 Available	31-May-01	31-Jul-01	31-Aug-01	Delayed (See #6)
Shells (Module #3) CUM #12 Available	31-May-01	31-Jul-01	31-Aug-01	Delayed (See #7)
Mangement Contingency Go-Ahead	2-Jul-01	2-Jul-01	2-Oct-01	Delayed (See #8)
Shells (Module #3) CUM #14 Available	31-Jul-01	31-Jul-01	1-Sep-01	Delayed (See #9)
Wire Joints -2 CUM #15 (200/m) Available	31-Jul-01	31-Jul-01	31-Aug-01	Delayed (See #10)
CUM #27,943 Available from CERN	31-Jul-01	31-Jul-01	31-Aug-01	Delayed (See #11)
CUM #42 Kit Available	31-Jul-01	31-Jul-01	31-Oct-01	Delayed (See #12)
HV Plates (Module #1) CUM #18 Available	31-Jul-01	31-Jul-01	1-Sep-01	Delayed (See #13)
HV Plates (Module #2) CUM #18 Available	31-Jul-01	31-Jul-01	1-Sep-01	Delayed (See #14)
HV Plates (Module #3) CUM #14 Available	31-Jul-01	31-Jul-01	31-Dec-01	Delayed (See #15)
Module Assy #1 IU Module Assy CUM #13 Complete	31-Jul-01	31-Jul-01	1-Sep-01	Delayed (See #16)
Module Assy #2 Duke Module Assy CUM #13 Complete	31-Jul-01	31-Jul-01	1-Sep-01	Delayed (See #17)
Module Assy #3 Duke & IU Module Assy CUM #8 Complete	31-Jul-01	31-Jul-01	1-Nov-01	Delayed (See #18)
Shells (Module #1) CUM #18 Available	31-Jul-01	31-Jul-01	1-Sep-01	Delayed (See #19)
Shells (Module #2) CUM #18 Available	31-Jul-01	31-Jul-01	1-Sep-01	Delayed (See #20)
CUM #20,665 Available from Hampton	31-Jul-01	31-Jul-01	31-Aug-01	Delayed (See #21)

Note #1-2 In production, but not here yet.
Note #3 American Circuits working on backlog of approved plates.
Note #4 Delayed due to pause.

Note #5-7 Shells are keeping up with production but are delayed WRT schedule.
Note #8 Delayed until October when our production rates will be clearer.
Note #9-21 Delayed.

1.2.5.1.2 Prototype

Milestone	Baseline	Previous	Forecast	Status
ASDBLR Design Frozen	13-Jul-01	13-Aug-01	15-Sep-01	Delayed (See #1)

Note #1 The new "properly processed" wafers arrived in mid July and plastic packaged parts were delivered on the 31st. Preliminary measurements indicate that matching and other functionality is as expected (hoped), however, the noise measurements are not as good as the SPice simulations would have indicated. There is something not yet understood about either the design or the process and we need to be sure that we understand where the excess noise is coming from and to what level we can tolerate somewhat more input noise before we can consider the design frozen. Until we have such an understanding we cannot be certain that some design changes will be necessary. The 15 Sept. date is merely a guess - were we to have confidence in our understanding anytime before mid November it would be unlikely to have any effect on the overall schedule as the PRR must wait for information from large scale tests before it can proceed and those tests will occupy several months.

1.2.5.1.3 Production (Qty = 64,000 + 32,000 Chips)

Milestone	Baseline	Previous	Forecast	Status
Management Contingency Go-Ahead	2-Jul-01	2-Jul-01	15-Aug-01	Delayed (See #1)

Note #1 We hope this is on schedule - sort of not entirely under our control though. - that was last month's statement. The schedule is still not under our control. Right now the increased noise leaves us uncertain about when we will actually be prepared to go forward with pre-production and production purchases, but if the contingency go-ahead is delayed much more, then we will certainly not be able to meet the ATLAS milestones or we will have to pay much more. We were recently notified that it was necessary that the project office "be aware of the overall chip yield" prior to any consideration of release of contingency - note that this was sent to us 28 days AFTER the project office stipulated date of contingency go-ahead. The yield numbers available to us (and the project office) have not changed over the last few months - still ~45% overall yield from the first and only wafer run - we will have numbers on the second wafer fab in the middle of August and they will almost certainly be better - probably above 80%, but the confidence in any of those numbers is fairly small as the number of lots is only two. The noise question confuses this a bit, but is mostly a question of how we balance what we can live with what we are willing to change - in the worst case we revert to the single stripe transistors and pare down the input protection system.

1.2.1 Barrel Mechanics

1.2.1.1 Barrel Module — Ken McFarlane (Hampton University)

See details below.

1.2.1.1.1 Design — Harold Ogren (Indiana University)

Design work on the cooling plates and the spaceframe continue in coordination with CERN. Computer design of a web site for displaying the three site data base is progressing well, and the work of keeping the databases current is on going and time consuming.

1.2.1.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
CUM #23,343 Available from CERN	28-Feb-01	--	28-Aug-01	Delayed (See #1)
HV Plates (Module #3) CUM #5 Available	28-Feb-01	--	28-Aug-01	Delayed (See #2)
Shells (Module #3) CUM #9 Available	28-Feb-01	--	28-Jul-01	Completed
HV Plates (Module #1) CUM #12 Available	30-Mar-01	--	30-Jul-01	Completed
HV Plates (Module #2) CUM #12 Available	30-Mar-01	30-Jul-01	30-Aug-01	Delayed (See #3)
HV Plates (Module #3) CUM #9 Available	30-Mar-01	30-Sep-01	30-Jul-01	Completed (See #4)
CUM #27 Kit Available	30-Apr-01	--	30-Sep-01	Delayed (See #5)
CUM #5 Test Complete	30-Apr-01	--	30-Sep-01	Delayed (See #6)
HV Plates (Module #1) CUM #14 Available	30-Apr-01	--	30-Jul-01	Completed (See #7)
HV Plates (Module #2) CUM #14 Available	30-Apr-01	30-Jul-01	30-Aug-01	Delayed (See #8)
HV Plates (Module #3) CUM #11 Available	30-Apr-01	--	30-Sep-01	Delayed (See #9)
Module Assy #1 IU Module Assy CUM #7 Complete	30-Apr-01	30-Aug-01	30-Jul-01	Completed
Module Assy #3 Duke & IU Module Assy CUM #3 Complete	30-Apr-01	--	30-Sep-01	Delayed (See #10)
CUM #32 Kit Available	31-May-01	--	1-Sep-01	Delayed (See #11)
CUM #9 Test Complete	31-May-01	--	1-Sep-01	Delayed (See #12)
HV Plates (Module #1) CUM #16 Available	31-May-01	--	1-Sep-01	Delayed (See #13)
HV Plates (Module #2) CUM #15 Available	31-May-01	--	1-Sep-01	Delayed (See #14)
HV Plates (Module #3) CUM #12 Available	31-May-01	--	31-Oct-01	Delayed (See #15)
Module Assy #1 IU Module Assy CUM #9 Complete	31-May-01	--	1-Sep-01	Delayed (See #16)
Module Assy #2 Duke Module Assy CUM #9 Complete	31-May-01	31-Jul-01	31-Aug-01	Delayed (See #17)
Module Assy #3 Duke & IU Module Assy CUM #4 Complete	31-May-01	--	1-Sep-01	Delayed (See #18)
Shells (Module #1) CUM #16 Available	31-May-01	31-Jul-01	31-Aug-01	Delayed (See #19)
Shells (Module #2) CUM #15 Available	31-May-01	31-Jul-01	31-Aug-01	Delayed (See #20)
Shells (Module #3) CUM #12 Available	31-May-01	31-Jul-01	31-Aug-01	Delayed (See #21)
CUM #37 Kit Available	29-Jun-01	--	29-Jun-02	Delayed (See #22)
HV Plates (Module #1) CUM #17 Available	29-Jun-01	--	29-Aug-01	Delayed (See #23)
HV Plates (Module #2) CUM #17 Available	29-Jun-01	--	29-Aug-01	Delayed (See #24)
HV Plates (Module #3) CUM #13 Available	29-Jun-01	--	29-Oct-01	Delayed (See #25)
Module Assy #1 IU Module Assy CUM #11 Complete	29-Jun-01	--	29-Sep-01	Delayed (See #26)

Module Assy #2 Duke Module Assy CUM #11 Complete	29-Jun-01	--	29-Sep-01	Delayed (See #27)
Module Assy #3 Duke & IU Module Assy CUM #6 Complete	29-Jun-01	--	29-Sep-01	Delayed (See #28)
Shells (Module #1) CUM #17 Available	29-Jun-01	--	29-Aug-01	Delayed (See #29)
Shells (Module #2) CUM #17 Available	29-Jun-01	--	29-Aug-01	Delayed (See #30)
Shells (Module #3) CUM #13 Available	29-Jun-01	--	29-Sep-01	Delayed (See #31)
CUM #18,200 Available from Hampton	30-Jun-01	--	30-Jul-01	Completed
CUM #25,643 Available from CERN	30-Jun-01	--	30-Aug-01	Delayed (See #32)
Mangement Contingency Go-Ahead	2-Jul-01	2-Jul-01	2-Oct-01	Delayed (See #33)
CUM #20,665 Available from Hampton	31-Jul-01	31-Jul-01	31-Aug-01	Delayed (See #34)
CUM #27,943 Available from CERN	31-Jul-01	31-Jul-01	31-Aug-01	Delayed (See #35)
CUM #42 Kit Available	31-Jul-01	31-Jul-01	31-Oct-01	Delayed (See #36)
HV Plates (Module #1) CUM #18 Available	31-Jul-01	31-Jul-01	1-Sep-01	Delayed (See #37)
HV Plates (Module #2) CUM #18 Available	31-Jul-01	31-Jul-01	1-Sep-01	Delayed (See #38)
HV Plates (Module #3) CUM #14 Available	31-Jul-01	31-Jul-01	31-Dec-01	Delayed (See #39)
Module Assy #1 IU Module Assy CUM #13 Complete	31-Jul-01	31-Jul-01	1-Sep-01	Delayed (See #40)
Module Assy #2 Duke Module Assy CUM #13 Complete	31-Jul-01	31-Jul-01	1-Sep-01	Delayed (See #41)
Module Assy #3 Duke & IU Module Assy CUM #8 Complete	31-Jul-01	31-Jul-01	1-Nov-01	Delayed (See #42)
Shells (Module #1) CUM #18 Available	31-Jul-01	31-Jul-01	1-Sep-01	Delayed (See #43)
Shells (Module #2) CUM #18 Available	31-Jul-01	31-Jul-01	1-Sep-01	Delayed (See #44)
Shells (Module #3) CUM #14 Available	31-Jul-01	31-Jul-01	1-Sep-01	Delayed (See #45)
Wire Joints -1 CUM #36 (600/m) Available	31-Jul-01	--	31-Jul-01	Completed
Wire Joints -2 CUM #15 (200/m) Available	31-Jul-01	31-Jul-01	31-Aug-01	Delayed (See #46)
CUM #1 Kit Available	31-Aug-01	--	31-Aug-01	On Schedule
CUM #23,000 Available from Hampton	31-Aug-01	--	31-Aug-01	On Schedule
CUM #30,243 Available from CERN	31-Aug-01	--	31-Aug-01	On Schedule
CUM #48 Kit Available	31-Aug-01	--	31-Aug-01	On Schedule
HV Plates (Module #1) CUM #20 Available	31-Aug-01	--	31-Aug-01	On Schedule
HV Plates (Module #2) CUM #19 Available	31-Aug-01	--	31-Aug-01	On Schedule
HV Plates (Module #3) CUM #15 Available	31-Aug-01	--	31-Aug-01	On Schedule
Module Assy #1 IU Module Assy CUM #15 Complete	31-Aug-01	--	31-Aug-01	On Schedule

Module Assy #2 Duke Module Assy CUM #15 Complete	31-Aug-01	--	31-Aug-01	On Schedule
Module Assy #3 Duke & IU Module Assy CUM #10 Complete	31-Aug-01	--	31-Aug-01	On Schedule
Shells (Module #1) CUM #20 Available	31-Aug-01	--	31-Aug-01	On Schedule
Shells (Module #2) CUM #19 Available	31-Aug-01	--	31-Aug-01	On Schedule
Shells (Module #3) CUM #15 Available	31-Aug-01	--	31-Aug-01	On Schedule
Wire Joints -1 CUM #40 (600/m) Available	31-Aug-01	--	31-Aug-01	On Schedule
Wire Joints -2 CUM #17 (200/m) Available	31-Aug-01	--	31-Aug-01	On Schedule
CUM #25,400 Available from Hampton	28-Sep-01	--	28-Sep-01	On Schedule
CUM #32,543 Available from CERN	28-Sep-01	--	28-Sep-01	On Schedule
CUM #54 Kit Available	28-Sep-01	--	28-Sep-01	On Schedule
HV Plates (Module #1) CUM #21 Available	28-Sep-01	--	28-Sep-01	On Schedule
HV Plates (Module #2) CUM #21 Available	28-Sep-01	--	28-Sep-01	On Schedule
HV Plates (Module #3) CUM #16 Available	28-Sep-01	--	28-Sep-01	On Schedule
Module Assy #1 IU Module Assy CUM #17 Complete	28-Sep-01	--	28-Sep-01	On Schedule
Module Assy #2 Duke Module Assy CUM #17 Complete	28-Sep-01	--	28-Sep-01	On Schedule
Module Assy #3 Duke & IU Module Assy CUM #12 Complete	28-Sep-01	--	28-Sep-01	On Schedule
Shells (Module #1) CUM #21 Available	28-Sep-01	--	28-Sep-01	On Schedule
Shells (Module #2) CUM #21 Available	28-Sep-01	--	28-Sep-01	On Schedule
Shells (Module #3) CUM #16 Available	28-Sep-01	--	28-Sep-01	On Schedule
Wire Joints -1 CUM #44 (600/m) Available	28-Sep-01	--	28-Sep-01	On Schedule
Wire Joints -2 CUM #19 (200/m) Available	28-Sep-01	--	28-Sep-01	On Schedule
CUM #25 Test Complete	30-Sep-01	--	31-May-02	Delayed (See #47)
Production Modules A Testing Complete	30-Sep-01	--	30-Sep-01	On Schedule
Shells (Module #3) CUM #10 Available	30-Sep-01	--	30-Sep-01	On Schedule
CUM #27,800 Available from Hampton	31-Oct-01	--	31-Oct-01	On Schedule
CUM #31 Test Complete	31-Oct-01	--	31-Oct-01	On Schedule
CUM #34,843 Available from CERN	31-Oct-01	--	31-Oct-01	On Schedule
CUM #60 Kit Available	31-Oct-01	--	31-Oct-01	On Schedule
HV Plates (Module #1) CUM #22 Available	31-Oct-01	--	31-Oct-01	On Schedule
HV Plates (Module #2) CUM #22 Available	31-Oct-01	--	31-Oct-01	On Schedule
HV Plates (Module #3) CUM #17 Available	31-Oct-01	--	31-Oct-01	On Schedule
Module Assy #1 IU Module Assy CUM #19	31-Oct-01	--	31-Oct-01	On Schedule

Complete				
Module Assy #2 Duke Module Assy CUM #19 Complete	31-Oct-01	--	31-Oct-01	On Schedule
Module Assy #3 Duke & IU Module Assy CUM #14 Complete	31-Oct-01	--	31-Oct-01	On Schedule
Modules Production A Complete	31-Oct-01	--	31-Oct-01	On Schedule
Shells (Module #1) CUM #22 Available	31-Oct-01	--	31-Oct-01	On Schedule
Shells (Module #2) CUM #22 Available	31-Oct-01	--	31-Oct-01	On Schedule
Shells (Module #3) CUM #17 Available	31-Oct-01	--	31-Oct-01	On Schedule
Wire Joints -1 CUM #48 (600/m) Available	31-Oct-01	--	31-Oct-01	On Schedule
Wire Joints -2 CUM #21 (200/m) Available	31-Oct-01	--	31-Oct-01	On Schedule
Wire Joints -1 CUM #100 (600/m) Available	29-Nov-01	--	29-Nov-01	On Schedule
CUM #1 Test Complete	30-Nov-01	--	30-Nov-01	On Schedule
CUM #30,100 Available from Hampton	30-Nov-01	--	30-Nov-01	On Schedule
CUM #37 Test Complete	30-Nov-01	--	30-Nov-01	On Schedule
CUM #37,143 Available from CERN	30-Nov-01	--	30-Nov-01	On Schedule
CUM #66 Kit Available	30-Nov-01	--	30-Nov-01	On Schedule
HV Plates (Module #1) CUM #24 Available	30-Nov-01	--	30-Nov-01	On Schedule
HV Plates (Module #2) CUM #23 Available	30-Nov-01	--	30-Nov-01	On Schedule
Module Assy #1 IU Module Assy CUM #21 Complete	30-Nov-01	--	30-Nov-01	On Schedule
Module Assy #2 Duke Module Assy CUM #21 Complete	30-Nov-01	--	30-Nov-01	On Schedule
Module Assy #3 Duke & IU Module Assy CUM #15 Complete	30-Nov-01	--	30-Nov-01	On Schedule
Shells (Module #1) CUM #24 Available	30-Nov-01	--	30-Nov-01	On Schedule
Shells (Module #2) CUM #23 Available	30-Nov-01	--	30-Nov-01	On Schedule
Shells (Module #3) CUM #18 Available	30-Nov-01	--	30-Nov-01	On Schedule
Wire Joints -1 CUM #52 (600/m) Available	30-Nov-01	--	30-Nov-01	On Schedule
Wire Joints -2 CUM #23 (200/m) Available	30-Nov-01	--	30-Nov-01	On Schedule
CUM #32,500 Available from Hampton	31-Dec-01	--	31-Dec-01	On Schedule
CUM #39,443 Available from CERN	31-Dec-01	--	31-Dec-01	On Schedule
CUM #43 Test Complete	31-Dec-01	--	31-Dec-01	On Schedule
CUM #71 Kit Available	31-Dec-01	--	31-Dec-01	On Schedule
HV Plates (Module #1) CUM #25 Available	31-Dec-01	--	31-Dec-01	On Schedule
HV Plates (Module #2) CUM #25 Available	31-Dec-01	--	31-Dec-01	On Schedule
HV Plates (Module #3) CUM #19 Available	31-Dec-01	--	31-Dec-01	On Schedule

Module Assy #2 Duke Module Assy CUM #22 Complete	31-Dec-01	--	31-Dec-01	On Schedule
Module Assy #3 Duke & IU Module Assy CUM #16 Complete	31-Dec-01	--	31-Dec-01	On Schedule
Shells (Module #1) CUM #25 Available	31-Dec-01	--	31-Dec-01	On Schedule
Shells (Module #2) CUM #25 Available	31-Dec-01	--	31-Dec-01	On Schedule
Shells (Module #3) CUM #19 Available	31-Dec-01	--	31-Dec-01	On Schedule
Wire Joints -1 CUM #56 (600/m) Available	31-Dec-01	--	31-Dec-01	On Schedule
Wire Joints -2 CUM #25 (200/m) Available	31-Dec-01	--	31-Dec-01	On Schedule

Note #1 Straws hve been shipped but are held up at CERN.
Note #2, 10, 25, 28 Delayed due to hold up in HV plates.
Note #3-4 In production, but not here yet.
Note #5 Successful shipment from Dubna.
Note #6 Testing at Hampton still not operational.
Note #7-8 American Circuits working on backlog of approved plates.
Note #9 HV plate 3 are delayed due to machining problems
Note #11-14, 16-18 Delayed due to pause.
Note #15 Delayed due to HV 3 plates.
Note #19-21 Shells are keeping up with production but are delayed WRTschedule.
Note #22 Kits will follow HV plates.
Note #23-24, 27, 29-32, 34-46 Delayed.
Note #26 Delayed due to pause and parts.
Note #33 Delayed until October when our production rates will be clearer.
Note #47 This appears to be out of sequence.

Ken McFarlane (Hampton University)

Staff
No change; we now have a total of 5 technicians (including the QA tech, who now does assembly work on tension plates and capacitor barrels).

1.2.1.1.3.1 Detector Elements
1.2.1.1.3.1.1 Straws
A shipment of straws has been requested, from JINR (Dubna)
1.2.1.1.3.1.1.2 End sockets (end plugs)
1.2.1.1.3.1.1.4.1 Twister
1.2.1.1.3.1.1.4.2 Twister
1.2.1.1.3.1.1.8.2 Wire bushing (eyelet)
1.2.1.1.3.1.1.8.3 Crimp pin (taper pin)
1.2.1.1.3.1.1.8.5, 6 Gas connections
All purchase orders or contracts for the above components have been placed, and deliveries are on schedule. Revised drawings for new gas connections were received.

1.2.1.1.3.4 Assembly

Straw subassemblies
1,831 straw subassemblies were completed, 2,330 shipped, leaving 865 in inventory.

Radiator packs
Two type-1, one type-2, and 2 type-3, radiator pack kits were produced this month.

Dividers
Two type-1, and one type-2, divider kits were produced this month.

Wire supports
4,897 outer wire supports were assembled this month. 5,991 were shipped, leaving none in inventory.

Capacitor Barrels
Produced as needed for tension-plate processing.

Tension plates
These are now processed as needed to create HV plate/TP kits.

HV plate testing and assembly with tension plates
Five HV plate/TP kits were produced (three type-1, one type-2, one type-3).

Capacitor Assembly
No activity this month. The final decision on capacitor type has not been made.

1.2.1.1.3.1.1.8.5, 6 Gas connections
Active gas fittings are produced as needed for TP/HV kits.

Seog Oh (Duke University)

X-ray Scanner

Because of the amplifier problem, we were not able to scan any modules for a month. There were two problems. One was the noise (oscillation) and the other was the input protection problem. To address the problems, we have designed and made PCB boards to mount the amplifiers. We have assembled and gone through the first test and the results are quite good. We should be able to resume the scanning this week.

One of the findings from the x-ray scan is that the straws at one corner exhibit somewhat large gain variations. This feature showed up in several modules and we are investigating the cause. We have checked the assembly fixture and alignment jig and found no problems. It is still a mystery.

Wire Joint aging study

One of the recommendations from the PAR is to proceed with the wire-joint aging test immediately. It has been shown that silicon can cause aging. Because there is silicon in glass, and silicon can be etched out by the florin radicals (the chamber gas contains CF4), the glass beads may promote aging. There are ~10 grams of glass beads in the entire barrel module. Although a preliminary study was performed a few years ago, a more systematic study was requested. We have finished to design and we are in the process of setting up the aging test. Because this will be a long-term test (~year), we have designed a system requires minimal human intervention.

For the test, we designed a module (~110 cm long) with 12 straws. These straws will be under intense radiation using ten 10 milli-cure SR90 sources. The test module is just finished and being tested. The rest of the components (like the stepping motor controlled Fe55 source holder and shields) are in hands and being assembled. We should be able to perform the first test early September. The DAQ and controller software is being worked on as well.

HV Plates

We are still in the process of understanding the type III problem. For some reason the plates attached to the front side of modules are meeting the specification while the ones in the back side do not. In order to isolate the problem, the vendor machined another 3 sets about half way (before the plates are flipped up for completing machining). The partially finished plates were measured and shown that they all met the spec. The plates were then returned to the vendor for the final machining. They are back to FNAL for the final measurement. It will be a few days before we receive the measurement. The status of the high voltage plates for type I and type II is good. The vendor is producing the rest of Type I sets (~25 sets). After Type I, Type II will be produced.

Module Construction Status

Module 2.08
This module is finished and waiting for the x-ray scan.

Module 2.09
The stringing is finished and going through the final HV and leak test.

Module 2.10
The mechanical construction has started

Module 3.02
The mechanical construction has started.

Wire-joint production
The wire-joint production is moving well. Both stations are producing high quality wire-joints. The number of joints produced is above LOB requirement.

Harold Ogren (Indiana University)

Divider material: Completed being assembled at Hampton

Radiator fiber punching

Radiator material of all types is almost complete at Breiner Co. There are only a several hundred mats of type 1 are still required. We are now doing a precise count of the number shipped, and the rejected mats (a few of type 3), so that we can finalize the contract. We will then write a follow up for the remaining mats needed for spares and waste. We have spare material at Breiner and at Bloomington to handle the extra radiator required.

Shells:
We received 6 shells from Vision this month, as required. We now are requesting that they focus on type 1, 2 for several months, to build up and inventory. Four of the shells were processed here and became final shell subassemblies.

Module production:

Module 1.01 Completed. Presently at Dubna, cooling after a radiation test. Indications so far are that no problems arose after approximately 20 LHC years of radiation.

Module 1.02 Completed. At Duke University for gain testing, still not started.

Module 1.03 Completed. Being prepared for shipment to Hampton University.

Module 1.04 Stringing completed, Initial HV testing and rework completed.

Module 1.05 Stringing completed, initial HV testing and rework completed

Module 1.06 Stringing completed. Initial HV testing and rework completed.

Module 1.07 stringing complete, Initial HV testing and rework completed.

Modules 1.08, 1.10 are being strung. 1.09 is awaiting stringing.

Module 1.11, 1.12, 1.13 being assembled and tested.

Module 3.01 has been strung, and is being tested.

The 16 channel tester from Duke has been tested and is close to being ready for a systematic survey of all wire tensions on completed modules.

The production cooling plate being prototyped and tested. We have a high pressure test set up almost complete for beinging a series of tests of several variations in the cooling plate design.

1.2.5 TRT Electronics
1.2.5.1 ASD/BLR
1.2.5.1.1 Design **Richard Van Berg (University Of Pennsylvania)**

No actual design work this month.

1.2.5.1.2 Prototype

Milestone	Baseline	Previous	Forecast	Status
ASDBLR Design Frozen	13-Jul-01	13-Aug-01	15-Sep-01	Delayed (See #1)
Select Final Electronic Design	31-Aug-01	--	31-Aug-01	On Schedule

Note #1 The new "properly processed" wafers arrived in mid July and plastic packaged parts were delivered on the 31st. Preliminary measurements indicate that matching and other functionality is as expected (hoped), however, the noise measurements are not as good as the SPice simulations would have indicated. There is something not yet understood about either the design or the process and we need to be sure that we understand where the excess noise is coming from and to what level we can tolerate somewhat more input noise before we can consider the design frozen. Until we have such an understanding we cannot be certain that some design changes will be necessary. The 15 Sept. date is merely a guess - were we to have confidence in our understanding anytime before mid November it would be unlikely to have any effect on the overall schedule as the PRR must wait for information from large scale tests before it can proceed and those tests will occupy several months.

Richard Van Berg (University Of Pennsylvania)

Further measurements were made on the "known bad" die and threshold matching is very good, response is slightly improved (as expected) and all functionality is ok. The tentative yield (very low statistics) now has no hit from parametric tests and so is much better than previously - nearly at the 90% level we might have expected from a MAXIM run. However, noise measurements indicate an ENC of nearly 4000 e rather than the Spice indicated 2100 e that was expected. These noise measurements were made on ceramic packaged chips so some of the increase is due to package effects that will not be present in TQFP or FBGA packages, but at least half of the increase is not explained this way and it constitutes a significant worry. Two major (well, major relative to this level of change - minor in most senses) changes in the design were made that could, conceivably, contribute to the increased noise:

1) the preamp input transistors were changed from simple single stripe devices to more normal multi-striped devices - in ordinary processes this change improves the noise figures.

2) additional resistance and diode structures were placed at the input to beef up the input protection. The increased resistance and added diode capacitance were expected to increase the noise somewhat, but that is included in the 2100 e figure. The other significant change, removing the zero tie point on the threshold reference is at the discriminator and cannot add to the noise. Further work is necessary to identify the cause and to design a proper response.

1.2.5.1.3 Production (Qty = 64,000 + 32,000 Chips)

Milestone	Baseline	Previous	Forecast	Status
Management Contingency Go-Ahead	2-Jul-01	2-Jul-01	15-Aug-01	Delayed (See #1)

Note #1 We hope this is on schedule - sort of not entirely under our control though. - that was last month's statement. The schedule is still not under our control. Right now the increased noise leaves us uncertain about when we will actually be prepared to go forward with pre-production and production purchases, but if the contingency go-ahead is delayed much more, then we will certainly not be able to meet the ATLAS milestones or we will have to pay much more. We were recently notified that it was necessary that the project office "be aware of the overall chip yield" prior to any consideration of release of contingency - note that this was sent to us 28 days AFTER the project office stipulated date of contingency go-ahead. The yield numbers available to us (and the project office) have not changed over the last few months - still ~45% overall yield from the first and only wafer run - we will have numbers on the second wafer fab in the middle of August and they will almost certainly be better - probably above 80%, but the confidence in any of those numbers is fairly small as the number of lots is only two. The noise question confuses this a bit, but is mostly a question of how we balance what we can live with what we are willing to change - in the worst case we revert to the single stripe transistors and pare down the input protection system.

1.2.5.2 DTM/ROC

1.2.5.2.1 Design **Richard Van Berg (University Of Pennsylvania)**

The only DTMROC design effort at the present time is that directed towards a deep submicron (DSM) version. The cells that Penn is responsible for have been delivered to CERN, the test chips with Ternary Receivers (and parts of the "front end") have been returned and tested - all is well. The project is going forward well with a probable submission time of October - this is not early, but is within reasonable schedule bounds and would give us information on the viability of the DSM option in time for a decision early in 2002.

1.2.5.2.2 Prototype **Richard Van Berg (University Of Pennsylvania)**

Eight "Good" wafers of DTMROCs (and ASDBLRs) version 00 were delivered to Penn in early July. Five wafers have been sent out for packaging in TQFPs. When those DTMROC devices return they will be run through automatic testing to determine yield and then good devices will be sent to CERN for inclusion on End Cap boards for system testing. For barrel use we are relying on using FBGA packages - a preliminary design for that package will be forwarded to Signetics for comment in early August.

1.2.5.3.1 Design **Richard Van Berg (University Of Pennsylvania)**

At present the End Cap board design is stable. The CERN group has already made the small modifications necessary to accept the 00 versions of the chips and should have boards before we can ship them tested chips. No surprises are expected, but the design will have to be tested.

1.2.5.3.2 Prototype **Richard Van Berg (University Of Pennsylvania)**

Recent tests at CERN using 384 channels of 99 version chips on triple flex and ASD boards continue to look very good in terms of noise and general operation. The 00 version silicon will be available shortly and those tests will be expanded and repeated. Radiation testing of the 99 version will also be done on the ASD and DTMROC boards presently assembled at CERN. No boards have yet been returned from testing, but neutron tests have started.

1.2.5.5 Beam Test

Milestone	Baseline	Previous	Forecast	Status
End of 01 Test Beam	28-Sep-01	--	4-Nov-01	Delayed (See #1)

Note #1 We have been granted additional time up through Nov. 4 01. This is a GOOD thing, and "delay" is to pejorative a term, but seems the only thing to pull down.

Richard Van Berg (University Of Pennsylvania)

Paul Keener spent ten days at CERN at the beginning of the month setting up and verifying the DAQ systems. All seems in good shape. Kristian Hahn has arranged his schedule to be available at CERN in August while Paul is on paternity stake out.

We are going to assemble one or more TB3 boards with new ASDBLR00's to be available for high rate single channel tests. Those boards will be shipped to CERN in early August.

1.2.5.6 System Integration & Installation

Milestone	Baseline	Previous	Forecast	Status
System Design Certified	1-Oct-01	--	1-Oct-01	On Schedule (See #1)

Note #1 This depends upon getting large enough system tests in place before Oct. and that depends upon getting enough chips from the Jan. submission and that depends upon getting wafers back and there is a glitch there, so hard to be sure that we can make this schedule, but not yet unreasonable - just tight and getting tighter. Also note that this only works for the End Cap, the Barrel milestone must be much later as it depends upon having an actual design in place and we are not there yet for the stamp boards.

Richard Van Berg (University Of Pennsylvania)

The ten barrel stamp boards shipped from Lund in June have been tested on the IMS tester and then "glop topped" to protect the bonding wires to the ASDBLRs. The initial yield is high, but the boards have no input protection installed and so there have been some channel casualties. Nevertheless, we have managed to get single stamp boards reading out through the miniRod/TTC system and, with some difficulty, have managed to get the same boards reading out through the module 2 snake cable and full length (10 meter) twisted pair cable. The next step is to get several stamp boards working at once on the snake cable and then assemble this to the detector and look for cosmic ray tracks.

One observations made during this initial turn on procedure was that the stamp boards are very much noisier than the same silicon on a TB3 or End Cap board. Examination of the traces to and from the ASDBLR die shows that there is a good deal of unavoidable crossing of input lines by outputs which is very likely the cause of the increased "noise" rate. Unfortunately, the topology is such that no chip on board solution is immune from such features - the FBGA packages, however, should provide sufficient linearization of the signal flow to allow more than adequate separation of inputs and outputs.

1.3 ARGON

Milestones with changed forecast dates:

1.3.2.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
2 Complete HV Feedthrough Ports	1-Mar-01	25-Jul-01	20-Jan-02	Delayed (See #1)
Barrel FTs (Mechanical) Delivered to CERN	1-May-01	15-Jul-01	20-Aug-01	Delayed (See #2)
Barrel FTs (Electrical) delivered to CERN	1-Jun-01	15-Jul-01	15-Sep-01	Delayed (See #3)
Production Complete	14-Sep-01	14-Sep-01	20-Jan-02	Delayed (See #4)

Note #1 The order of installation of HV and signal FT has been changed. HV cables will be installed after completion of signal FT installation.

Note #2-3 The delivery will match the installation program.

Note #4 The order of installation of HV and signal FT has been changed. HV cables will be installed after completion of signal FT installation.

1.3.2.2.4 Installation

Milestone	Baseline	Previous	Forecast	Status
Ship End-Cap C to CERN	5-Mar-01	25-Jul-01	20-Aug-01	Delayed (See #1)
Ship Barrel to CERN	1-May-01	1-Aug-01	20-Aug-01	Delayed (See #2)
Barrel Install Complete	1-Nov-01	1-Nov-01	20-Jan-02	Delayed (See #3)
Installation HVFT on Endcap C complete (Cables)	20-Feb-02	25-Nov-01	20-Jan-02	Delayed (See #4)

Note #1-2 Shipment combined with signal FT.

Note #3-4 The order of installation of HV and signal FT has been changed. HV cables will be installed after completion of signal FT installation.

1.3.3.1.2 LN2 Ref. System Procurement

Milestone	Baseline	Previous	Forecast	Status
Proposal Assessment & Contract Start	1-Feb-01	10-Jul-01	20-Aug-01	Delayed (See #1)
LN2 Ref. System Procurement Complete	2-Apr-01	15-Jul-01	20-Aug-01	Delayed (See #2)
Start Production	1-Aug-01	1-Aug-01	3-Sep-01	Delayed (See #3)

Note #1-2 Bids are higher than expected. Negotiations continue.

Note #3 Design and construction start one week after contract signing.

1.3.3.1.3 LN2 Ref. System Fabrication

Milestone	Baseline	Previous	Forecast	Status
LN2 Ref. System Fabrication Start	1-Jun-01	1-Aug-01	20-Aug-01	Delayed (See #1)

Note #1 Delay is due to price negotiations and paperwork related to purchase order. Not on a critical path.

1.3.3.2.2 Quality Meter Prototype

Milestone	Baseline	Previous	Forecast	Status
Final Design Review	1-May-01	21-Aug-01	15-Dec-01	Delayed (See #1)
Specification PRR Review	1-Aug-01	1-Aug-01	15-Dec-01	Delayed (See #2)

Note #1 Will match the cryostat installation schedule,

Note #2 The prototype exist. An improved design with higher reliability is under development.

1.3.3.2.3 Quality Meter Production

Milestone	Baseline	Previous	Forecast	Status
Parts and Material Start	29-Aug-01	29-Aug-01	15-Jan-02	Delayed (See #1)
Quality Meter Production	1-Oct-01	30-Oct-02	30-Jun-02	Delayed (See #2)
Assembly Start	26-Dec-01	26-Dec-01	26-Jun-02	Delayed (See #3)
Tests and calibration Start	26-Dec-01	26-Dec-01	26-Dec-02	Delayed (See #4)
Machining and Welding Start	26-Dec-01	26-Dec-01	26-Jun-02	Delayed (See #5)
Parts and Material Complete	28-Dec-01	28-Dec-01	28-Aug-02	Delayed (See #6)

Note #1-6 xx
Note #2 Delay matches the new ATLAS schedule.

1.3.4.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
Delivery of Module 7 boards	15-Jul-01	15-Jul-01	20-Aug-01	Delayed (See #1)
25% MB System Production Complete	6-Aug-01	6-Aug-01	31-Aug-01	Delayed (See #2)
Last Delivery of SB & MB PC Boards	1-Dec-01	1-Dec-01	1-Feb-02	Delayed (See #3)

Note #1 Delay due to motherboard 1-month hold because of ATLAS low profile connector problem. Motherboard production taken off hold and Module 7 will ship August 20, 2001.
Note #2 Delay due to motherboard 1-month hold because of ATLAS low profile connector problem. Motherboard production taken off hold.
Note #3 Vendor quality problems that have now been resolved.

1.3.5.2.3 Production Support to LAPPL/LAL

Milestone	Baseline	Previous	Forecast	Status
Production Readiness Review	1-May-01	1-Aug-01	20-Aug-01	Delayed (See #1)

Note #1 Delay in DMILL chip production.

1.3.7.1.2 Pre-Proto/Mod 0/Atlas Prototype

Milestone	Baseline	Previous	Forecast	Status
Freeze Connector Location	1-May-01	1-Jul-01	1-Sep-01	Delayed (See #1)
1st Delivery of Layer Sum Boards	2-Jul-01	2-Jul-01	1-Jan-02	Delayed (See #2)

Note #1 Delayed due to delay in finalizing TTC connector.
Note #2 Delayed until boards are needed for rad-tol FEB production.

1.3.9.1.1 Design

Milestone	Baseline	Previous	Forecast	Status
Reconstruct E, T, and chi square for TB data	12-Feb-01	1-Jul-01	1-Nov-01	Delayed (See #1)

Note #1 Done, not completely reviewed.

1.3.1 Barrel Cryostat

1.3.1.5 Assembly & Test in West Hall

Milestone	Baseline	Previous	Forecast	Status
Cryostat Arrives at CERN	15-May-01	--	15-Jul-01	Completed
Final Cryostat Acceptance (KHI-CERN)	31-Aug-01	--	31-Aug-01	On Schedule
Calorimeter Support Structure Complete	31-Oct-01	[New]	31-Oct-01	On Schedule
Cryo Line Installation Test Complete	31-Jul-02	[New]	31-Jul-02	On Schedule
Final Acceptance Test in West Area	30-Jun-03	[New]	30-Jun-03	On Schedule

Jack Sondericker (Brookhaven National Lab.)

July 2001 Barrel Cryostat Monthly Report

The Barrel Cryostat arrived at CERN on July 3rd, as scheduled. It was unloaded in the West Hall, protective shipping material removed and positioned in the testing area.

The final acceptance test began by first, a visual inspection which found no damage and reading of four internal position transducers that measure relative position of the cold vessel with respect to the warm. Readings were within allowable limits so the X and Z alignment of the cold vessel is the same as in Japan.

Pumps were mounted to the vacuum tank and after a day leak checking commenced. The cold vessel was pumped out and back filled with helium. No leak signal found on the $1x10^{-9}$ mbar.l/s range. Leak check of the Warm vacuum vessel revealed a crushed "O" ring on a feed thru blankoff flange (repaired) and a small leak in a fillet weld of the chimney.

Presently, discussions are on going with Kawasaki, CERN and BNL to come to agreement on how best carry out the repair.

1.3.2 Feedthrough

1.3.2.1 FT-Signal

1.3.2.1.1 Design

Milestone	Baseline	Previous	Forecast	Status
I/F Equipment Avail for Final Cryostat Complete	3-Sep-01	--	3-Sep-01	On Schedule

1.3.2.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
Last Pin Carrier Delivery	1-Mar-01	--	1-Sep-01	Delayed (See #1)
50% of Pin Carriers Delivered	2-Jul-01	--	2-Jul-01	Completed
34 FT Complete	15-Oct-01	--	15-Oct-01	On Schedule
54 FT Complete	17-Dec-01	--	17-Dec-01	On Schedule

Note #1 After initial delay, the production matches the new ATLAS schedule

Bob Hackenburg (Brookhaven National Lab.)

We are now working on feedthrough 28; production slowed a little this month with vacations and two feedthroughs which had to be cut open and repaired. The latest two problems appear to stem from the lack of side-pressure on the vacuum cables during their electrical tests; they failed only when installed and cold. We now use parallel clamps on the sides of the vacuum connectors while testing vacuum cables, to simulate the actual pressure they see when installed; these connectors are a little too fat, and make a very tight fit when installed.

We have also just shipped our first four feedthroughs to CERN.

1.3.2.1.4 Installation

Milestone	Baseline	Previous	Forecast	Status
Installation	17-Jan-01	--	30-Sep-02	Delayed (See #1)
1st Shipment	23-Apr-01	--	30-Jul-01	Completed
Start Installation Procedure	13-Jul-01	--	15-Sep-01	Delayed (See #2)
Last Shipment	31-Oct-01	--	30-Aug-02	Delayed (See #3)

Note #1 The completion date matches new ATLAS schedule.

Note #2 Installation cannot start before the acceptance tests of the cryostat are complete.

Note #3 The last shipment date matches the new ATLAS schedule. Feedthrough production will be completed earlier.

1.3.2.2 HV Feedthrough

1.3.2.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
2 Complete HV Feedthrough Ports	1-Mar-01	25-Jul-01	20-Jan-02	Delayed (See #1)
Barrel FTs (Mechanical) Delivered to CERN	1-May-01	15-Jul-01	20-Aug-01	Delayed (See #2)
Barrel FTs (Electrical) delivered to CERN	1-Jun-01	15-Jul-01	15-Sep-01	Delayed (See #3)
Production Complete	14-Sep-01	14-Sep-01	20-Jan-02	Delayed (See #4)

Note #1, 4 The order of installation of HV and signal FT has been changed. HV cables will be installed after completion of signal FT installation.

Note #2-3 The delivery will match the installation program.

For M. Rijssenbeek: **Richard Stroynowski (Southern Methodist University)**

1.3.2.2.3 Production

1.3.2.2.3.1 Warm Connectors

REDEL/LEMO warm HV connectors will start being mounted in mid-August.

1.3.2.2.3.2 Cold Connectors

Cold connectors will start being mounted in mid-August.

1.3.2.2.3.3 HV Wire

All wire has been received and used for manufacture of wire feedthroughs.

1.3.2.2.3.6 Sealed Wire FT (WFT)

Douglas Engineering has delivered all 28 WFTs (includes spares).

All WFTs have been HV tested in water and any faulty wires were removed (cut at the feedthrough). The final cleaning of all 28 WFTs was completed: first pass was water rinse, followed by a 3-8 hr soaking in an ultrasonic bath at 30-60 degrees C. The bath was filled with a 5% cleaning fluid (detergent) and water mix. The WFT was subsequently brushed over its full length in a tub filled with water, detergent and 10% alcohol. After rinsing the WFT was left to soak in a 30-40% Alcohol plus water mix for 3-8 hrs. The WFTs were then spread out in the cleanroom on nylon suspended nets, and given a final wipe down of the individual wires with 100% Alcohol and Kim-wipes. The wipes were inspected after each pass until no visible residue could be seen. The number of passes per wire varied between 2 and 10, with an average hovering between 3-4. We have set up and tested a procedure to start grouping HV wires into bundles (of 7 or 8 wires per bundle for the LArg Barrel). These bundles are selected such as to group nearest-neighbor wires into the same bundle, in order to minimize potential voltage differentials between neighboring wires in the feedthrough and the gas. After the full FT plate (4 WFTs) has been bundled, warm (first) and cold (second) connectors will be mounted. Bundling will start week of Aug 13.

1.3.2.2.3.4-5 Filter Modules and Filter Crate

All HV parts have been delivered.

1.3.2.2.3.7-9 Vacuum Components for the High Voltage Feedthrough (HVFT)

All six HVFTs (flanges, bellows, pipe, ALU/SS transitions) have been received, machined, and have been welded and tested at BNL. Numbers four to eight FT reducers (for the LArg EndCap and spare) are awaiting post-welding machining, where a delay has occurred because of vacations.

We have constructed two shipping crates, one of which will be used to ship the first mechanical HVFT to CERN (with the second shipment of BNL signal FTs - foreseen for mid-August). The HVFT will be suspended in foamed polyurethane packaging, which will be done at a local company. The FT will be covered in a polyethylene bag, and the bellows section (Cold pipe, bellows, transition metal, and the temporary end-flange are protected inside a capped PVC pipe, which is bolted onto the warm bolt flange.

1.3.2.2.3.10 Assembly

The first Barrel HVFT passed all HV and leak tests. The second Barrel HVFT will be tested after connectorizing and insertion of the wire tree through the HVFT cold pipe.

1.3.2.2.4 Installation

The current plans call for the installation of the Barrel HVFT before Signal FTs (as in the original plan) in mid-September, and to install the HV cable tree and do the routing when all welding has been done, and after cleaning of the cryostat (i.e. with the signal FT cables in place). The latter, second, phase of installation is foreseen for early January 2002.

Discussion and R&D on the proper cable ties/fasteners to use to suspend the cable tree off the 138 M5x6 blind bolt holes in the cold cryostat is ongoing.

1.3.2.2.4 Installation

Milestone	Baseline	Previous	Forecast	Status
Ship End-Cap C to CERN	5-Mar-01	25-Jul-01	20-Aug-01	Delayed (See #1)
Ship Barrel to CERN	1-May-01	1-Aug-01	20-Aug-01	Delayed (See #2)
Installation HVFT ports on Endcap C	5-Sep-01	--	25-Nov-01	Delayed (See #3)
Barrel Install Complete	1-Nov-01	1-Nov-01	20-Jan-02	Delayed (See #4)
Installation HVFT on Endcap C complete (mechanical)	1-Nov-01	[New]	1-Nov-01	On Schedule
Installation HVFT on Endcap C complete (Cables)	20-Feb-02	25-Nov-01	20-Jan-02	Delayed (See #5)
Install HVFT on Endcap A complete	28-Feb-02	[New]	28-Feb-02	On Schedule

(Cables)				
Install HVFT on Endcap A complete (mechanical)	28-Feb-02	[New]	28-Feb-02	On Schedule

Note #1-2 Shipment combined with signal FT.

Note #3 Delay will match the cryostat availability.

Note #4-5 The order of installation of HV and signal FT has been changed. HV cables will be installed after completion of signal FT installation.

1.3.3 LAr Cryogenics

1.3.3.1 LN2 Refrigerator System

1.3.3.1.2 LN2 Ref. System Procurement

Milestone	Baseline	Previous	Forecast	Status
Proposal Assessment & Contract Start	1-Feb-01	10-Jul-01	20-Aug-01	Delayed (See #1)
LN2 Ref. System Procurement Complete	2-Apr-01	15-Jul-01	20-Aug-01	Delayed (See #2)
Start Production	1-Aug-01	1-Aug-01	3-Sep-01	Delayed (See #3)

Note #1-2 Bids are higher than expected. Negotiations continue.

Note #3 Design and construction start one week after contract signing.

July 2001 LN2 Refrigerator Procurement **Jack Sondericker (Brookhaven National Lab.)**

Best and Final Offers were received by July 3rd as scheduled. After a week or so delay because of meetings and travel, the Source Selection Board met to review and score the technical proposals. The proposer with the highest technical score was also the lower cost, so making a winning decision was simple.

Presently, all the required paper work is being generated in support of the selection as required by US government rules. Announcement of the placement of order should be made during Mid August.

1.3.3.1.3 LN2 Ref. System Fabrication

Milestone	Baseline	Previous	Forecast	Status
Ln2 Ref. System Fabrication	1-Jun-01	--	1-Sep-03	Delayed (See #1)
LN2 Ref. System Fabrication Start	1-Jun-01	1-Aug-01	20-Aug-01	Delayed (See #2)

Note #1 The completion date of system installation matches new ATLAS installation schedule.

Note #2 Delay is due to price negotiations and paperwork related to purchase order. Not on a critical path.

1.3.3.2 LN2 Quality Meter System

1.3.3.2.2 Quality Meter Prototype

Milestone	Baseline	Previous	Forecast	Status
Quality Meter Prototype	1-May-00	--	21-Aug-01	Delayed (See #1)
Final Design Review	1-May-01	21-Aug-01	15-Dec-01	Delayed (See #2)
Specification PRR Review	1-Aug-01	1-Aug-01	15-Dec-01	Delayed (See #3)

Note #1, 3 The prototype exists. An improved design with higher reliability is under development.

Note #2 Will match the cryostat installation schedule.

July 2001 Quality Prototype **Jack Sondericker (Brookhaven National Lab.)**

During the month of July the mechanical design of the detector was optimized and the QW Meter electronics finalized. By mid July a multilayer printed circuit board was ordered for prototype testing. Delivery promised by August 1st. All electronic parts necessary for proto testing are on hand.

Mechanical parts for prototype testing are also on hand. The LN2 testing box was lengthened to accommodate an increase in detector overall length to increase sensitivity and relative stability.

Prototype testing should start by mid August which is on schedule.

1.3.3.2.3 Quality Meter Production

Milestone	Baseline	Previous	Forecast	Status
Parts and Material Start	29-Aug-01	29-Aug-01	15-Jan-02	Delayed (See #1)
Quality Meter Production	1-Oct-01	30-Oct-02	30-Jun-02	Delayed (See #2)
Assembly Start	26-Dec-01	26-Dec-01	26-Jun-02	Delayed (See #3)
Machining and Welding Start	26-Dec-01	26-Dec-01	26-Jun-02	Delayed (See #4)
Tests and calibration Start	26-Dec-01	26-Dec-01	26-Dec-02	Delayed (See #5)
Parts and Material Complete	28-Dec-01	28-Dec-01	28-Aug-02	Delayed (See #6)

Note #1, 3-6 xx

Note #2 Delay matches the new ATLAS schedule.

1.3.4 EM Electronics/MB System

1.3.4.2 Motherboard System

1.3.4.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
Delivery of Module 5 boards	1-Jun-01	--	1-Jun-01	Completed
Delivery of Module 6 boards	20-Jun-01	--	20-Jun-01	Completed
Delivery of Module 7 boards	15-Jul-01	15-Jul-01	20-Aug-01	Delayed (See #1)
25% MB System Production Complete	6-Aug-01	6-Aug-01	31-Aug-01	Delayed (See #2)
Delivery of Module 8 boards	1-Sep-01	[New]	1-Sep-01	On Schedule
Last Delivery of SB & MB PC Boards	1-Dec-01	1-Dec-01	1-Feb-02	Delayed (See #3)
50% MB System Production Complete	2-Dec-01	--	2-Dec-01	On Schedule

Note #1 Delay due to motherboard 1 month hold because of ATLAS low profile connector problem. Motherboard production taken off hold and Module 7 will ship August 20, 2001.

Note #2 Delay due to motherboard 1 month hold because of ATLAS low profile connector problem. Motherboard production taken off hold.

Note #3 Vendor quality problems that have now been resolved.

Srini Rajagopalan (Brookhaven National Lab.)

Module 13: completed, packed, shipped to Saclay on May 3, 2001.

Module 12: completed, packed, shipped to Annecy on May 6, 2001.

Module 11: completed, packed, shipped to Saclay on May 31,2001.

Module 10: completed, packed, shipped to Annecy on July 11,2001.

Module 9: Target ship date August 10,2001.

Summing Boards: All boards received, inspected and tested.

High Voltage Board: Boards received, inspected and in test.

Front Mother Boards: All boards received, inspected, and tested.

Back Mother Boards: All boards received, inspected, and tested.

Alignment Boards: In BNL stock.

Module 8: Target ship date September 1, 2001.

Summing Boards: All boards received, inspected and in test.

High Voltage Board: Boards received, inspected and in test.

Front Mother Boards: All boards received, inspected, and tested.

Back Mother Boards: All boards received, inspected, and tested.

Alignment Boards: In BNL stock.

Saclay reported continuity problems on a few motherboards. BNL is investigating the problem.

Impact of electrostatic discharges in the calorimeter on the calibration resistive networks being investigated at BNL

1.3.4.2.4 Installation Complete **Srini Rajagopalan (Brookhaven National Lab.)**

Saclay: M15, M13 stacked, cabled - complete

M13 in test beam

M11 being cabled

Annecy: M14 stacked and cabled - complete

M12 stacked awaiting to be cabled

M10 stacked, front face cabling complete

CERN: M6 to be stacked and cabled in September.

1.3.5 Preamp/Calibration

1.3.5.1 Preamps

1.3.5.1.3 Production (QTY=30000)

Milestone	Baseline	Previous	Forecast	Status
Start Preamp Deliveries to FEB	3-Sep-01	--	3-Sep-01	On Schedule

Hong Ma (Brookhaven National Lab.)

IO-826: received 1056 from vendor since last report. All in the process of being tested.

Total: 2112 received. 1043 passed and ready for shipment.

IO-824: Received none from vendor this month.

Total: 1152 received. 1147 passed and ready for shipment.

IO-823: Received 960 from vendor since last report.

Total: 5056 received. 96 test in progress. 4855 passed and ready for shipment.

Vendor delivered a total of 8,029 hybrids of which 2,016 hybrids delivered in the past four weeks. Production is 27% complete. The yield is 98.7% to 99.5%.

Both test stations are in operation.

1.3.5.2 Precision Calor. Calibration

1.3.5.2.3 Production Support to LAPPL/LAL

Milestone	Baseline	Previous	Forecast	Status
Production Readiness Review	1-May-01	1-Aug-01	20-Aug-01	Delayed (See #1)

Note #1 Delay in DMILL chip production

1.3.6 System Integration

1.3.6.1 Pedestal

1.3.6.1.1 Design **Helio Takai (Brookhaven National Lab.)**

Pedestal design -

We are adding a filter box for the pedestal services. The prototype filter is now concluded and it will be shipped to Kosice where it is going to be built.

1.3.6.1.2 Prototype **Helio Takai (Brookhaven National Lab.)**

The first article of barrel pedestal is in BNL and was mounted in the mockup. It looks good.

1.3.6.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
Start Barrel Pedestal Delivery to CERN	31-Dec-01	--	31-Dec-01	On Schedule
Start EC Pedestal Delivery to CERN	31-Dec-01	--	31-Dec-01	On Schedule
Start Ped.s deliveries Ship In Place	31-Dec-01	--	31-Dec-01	On Schedule

Helio Takai (Brookhaven National Lab.)

To start production we are awaiting details on the attachment holes for the filter box.

1.3.6.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
80% Warm Cables Delivered	28-Dec-01	--	28-Dec-01	On Schedule
80% Warm Cables Ship in Place	28-Dec-01	--	28-Dec-01	On Schedule
10% Deliveries Complete	31-Dec-01	--	31-Dec-01	On Schedule
10% Deliveries Ship in Place	31-Dec-01	--	31-Dec-01	On Schedule
1st Delivery Date to CERN	31-Dec-01	--	31-Dec-01	On Schedule
1st Delivery Ship in Place	31-Dec-01	--	31-Dec-01	On Schedule

1.3.6.3 Crate-Mechanical

1.3.6.3.1 Design — Helio Takai (Brookhaven National Lab.)

The design of the crate is concluded.

1.3.6.3.2 Prototype — Helio Takai (Brookhaven National Lab.)

The first article is in BNL. We have mounted on the mockup and it is now being used regularly. The mechanics checks with the design. Production is awaiting the pedestal design to be concluded and checked.

1.3.6.4 Power and Services

1.3.6.4.1 Design — Helio Takai (Brookhaven National Lab.)

The Anderson connector termination for bus bars is now being used in the mockup at BNL. This termination is better than the previous ODU connector. It is much harder to install, difficult to handle, and very very difficult to disconnect, qualities which seem appropriate for where it is going to be used.

1.3.6.4.2 Prototype — Helio Takai (Brookhaven National Lab.)

A prototype power supply is now ready. We have discussed with Modular Devices the delivery of 10 units just like the prototype, except with FET in die format. These 10 units will be subjected to radiation and magnetic field tests.

The prototype has a remarkable flat efficiency as function of the output load. Noise figures are typical of switching power supplies without filter.

A schedule for using accelerators for testing has been established and it will take us about 2-3 months for evaluation of the power supplies.

1.3.6.5 Cooling

1.3.6.5.1 Design — Helio Takai (Brookhaven National Lab.)

The design of the cooling plate needs to be re-evaluated, from both mechanical and electrical point of view. The prototypes fabricated by Showa Aluminum seem to fit the bill. However the pressure drop seems to be slightly higher than previous prototypes. A higher pumping volume may be required if the present design is adopted.

1.3.6.5.2 Prototype — Helio Takai (Brookhaven National Lab.)

Prototypes made by Showa Aluminum is being tested now for 2 months for corrosion. No signs of oxidation or corrosion are seen. We are therefore confident that these will survive the required 10yrs of operation.

1.3.6.5.3 Production

Milestone	Baseline	Previous	Forecast	Status
Cooling Liquid Decision	17-Dec-01	--	17-Dec-01	On Schedule

1.3.7 Front End Board

1.3.7.1 FEB

1.3.7.1.1 Design — John Parsons (Columbia University)

Functional testing was successfully performed of the 3 new DSM ASICs (SCA Controller, Gain Selector, CLKFO). All 3 designs function as anticipated. Preparations were completed for the irradiation testing of the first two on July 28/29 (see the report below). The final technology decision (DMILL or DSM) will be made in October for these chips.

Design of the FEB continued. We are investigating how to implement the first FEB before the STm rad-tol regulators are available, so that we can use the first FEB for tests of analog and digital functionality and then later retrofit it with rad-tol regulators once they are available.

We continue studies of backup solutions to the STm regulators, including commercial rad-tol regulators and solutions constructed using commercial parts. Initial radiation tests (see report below) are not very encouraging.

1.3.7.1.2 Pre-Proto/Mod 0/Atlas Prototype

Milestone	Baseline	Previous	Forecast	Status
Freeze Component for ATLAS Prototype	1-Mar-01	--	1-Aug-01	Delayed (See #1)
Freeze Connector Location	1-May-01	1-Jul-01	1-Sep-01	Delayed (See #2)
Rad Tol. FEB Design Review	1-May-01	--	3-Sep-01	Delayed (See #3)
1st Delivery of Layer Sum Boards	2-Jul-01	2-Jul-01	1-Jan-02	Delayed (See #4)
Feb - ATLAS Layout Complete	21-Aug-01	--	21-Aug-01	On Schedule
Critical Design Review	3-Sep-01	--	3-Sep-01	On Schedule
Start Assembly	11-Sep-01	--	11-Sep-01	On Schedule
Rad Hard. - All Components	28-Sep-01	--	28-Feb-02	Delayed (See #5)
Final Dec. DMILL/IBM	7-Dec-01	--	7-Dec-01	On Schedule

Note #1 Delayed due to requirement for additional radiation testing of COTs.

Note #2 Delayed due to delay in finalizing TTC connector.

Note #3, 5 Delayed due to late delivery of rad-tol voltage regulators.

Note #4 Delayed until boards are needed for rad-tol FEB production.

1.3.7.1.5 Radiation Testing **John Parsons (Columbia University)**

On July 28/29, we performed p-irradiation tests of several different types of components:

1. DSM ASICs (SCA Controller, Gain Selector)

- no degradation was seen with total dose

- active monitoring revealed a low rate of SEU in the logic and, particularly, in the RAM of the SCA Controller. Analysis of the data continues, but it is already clear the rate of errors implied for operation in ATLAS is acceptably small.

2. Voltage regulators

- we irradiated several commercial regulators, selected from Omnirel, Intersil, and National

- all showed significant damage at relatively low doses, except for the HS9S-117RH from Intersil, a rad-hard component offered (in small quantities) at about $70 per piece

- further analysis of the data continues, and a more detailed report will be prepared.

We have booked Harvard again for the weekend of Aug. 18/19 for the next set of irradiation tests.

1.3.7.2 SCA

1.3.7.2.1 Design — John Parsons (Columbia University)

The final two wafers from the engineering run were delivered and the chips packaged. They were testing using the robotic test system at Grenoble. The resulting measurements were recorded to a database, which will be analyzed in setting the final selection criteria. Initial yield estimates are approx. 60-70%.

The PRR is expected in October, and will be immediately followed by the launch of production.

1.3.7.4 Optical Links

1.3.7.4.1 Design — John Parsons (Columbia University)

Work continues with our Taiwanese colleagues on the final link implementation.

1.3.7.4.2 Prototype/Module 0

Milestone	Baseline	Previous	Forecast	Status
Optical Links ATLAS Prototype	1-Jun-01	--	1-Jun-02	Delayed (See #1)

Note #1 Prototype completed and tested. FEB-end integrated with the layout. ROD-end will depend on the ROD design.

1.3.8 Trigger Summation

1.3.8.1 Layer Sums

1.3.8.1.2 Prototype-Lay Sum Boards/Electronics — Bill Cleland (University Of Pittsburgh)

During the month of July, the testing of LSBs continued apace. We are still seeing a failure rate of about 3%, and we are now making categories of failures and learning how to rework the problem boards. None of the problems found so far seem insurmountable. We continue to work on the plan to rework the S1x16 gain 2 boards described in the previous report.

1.3.8.1.3 Production (Qty = 3,441 Boards)

Milestone	Baseline	Previous	Forecast	Status
Last Delivery of Layer Sum Bds	1-Jul-01	--	1-Jul-01	Completed
Start Deliveries to FEB (ORSAY/Nevis)	2-Jul-01	--	1-Jan-02	Delayed (See #1)

Note #1 Delivery will be started to Nevis or Orsay only when requested.

1.3.8.2 Interface to Level 1

1.3.8.2.1 Design/Electronic Tooling/Comp. Specs

Milestone	Baseline	Previous	Forecast	Status
Circuit Design of ATLAS receiver Complete	12-Aug-01	--	12-Sep-01	Delayed (See #1)
Final Design Complete	4-Oct-01	--	4-Oct-01	On Schedule (See #2)
Critical Design Review	12-Dec-01	--	12-Dec-01	On Schedule (See #3)

Note #1 The choice for the variable gain amplifier IC for the receiver is being revisited. We are examining the possibility of using a fast DAC as a variable attenuator as an alternative. Two DACs of the required bandwidth have been located, and we are making evaluation boards to look at them.

Note #2 It is likely that this milestone will be missed by a month or so, due to the delay arising from the study of the variable gain amplifier mentioned above.

Note #3 This milestone may slip if the production of the prototype is delayed.

Bill Cleland (University Of Pittsburgh)

Work on the receiver system is continuing. We have now produced prototype daughterbaords for the complete analog chain, and we are setting up a test bench to look at them in detail. We will be joined in this effort by Jeff McDonald, who is a welcome addition to our team. We are looking for ways to achieve a variable gain amplifier with lower noise than is found in the commercially available voltage-controlled amplifier chips. We have located two multiplying DACs with sufficient bandwidth to handle our signal, but we must make some small evaluation boards to measure the noise and check their suitability for our application. Once that is done, a redesign of the VGA daughterbaord can begin.

1.3.9 ROD System

1.3.9.1 ROD Board

1.3.9.1.1 Design

Milestone	Baseline	Previous	Forecast	Status
Reconstruct E, T, and chi square for TB data	12-Feb-01	1-Jul-01	1-Nov-01	Delayed (See #1)
Complete Code to form averages of Cal.	18-Jun-01	--	1-Sep-01	Delayed (See #2)
Complete Code to get OFC from CAL. Data	4-Sep-01	--	4-Sep-01	On Schedule (See #3)
Real time evaluation of optimal filter coeff.	3-Dec-01	--	3-Dec-01	On Schedule (See #4)

Note #1 Done, not completely reviewed.

Note #2-3 Calibration procedure not completely defined.

Note #4 Simulations for the new TI C64 DSP are under way.

Rod Engelmann (SUNY Stony Brook)

In June the following work was done:

BNL/Stony Brook - ROD demo tests: Work with the calibration board and the trigger analyzer board continued. Preparations for the new FEB board were made.

Nevis Lab: Performance studies with the 6203 PU were continued and reported in the July 10 ROD Technical Meeting: energy, time and chi squared for 128 channels are calculated in 5.8 microseconds. Input/output of the data is now the bottleneck with 10 microseconds needed. Work on simulation of the new TI C64 DSP was begun and is well under way.

SMU: Code development for averaging calibration data in the TI C62 DSP continued. The TI Code Composer software was successfully set up and run with the existing C6202 code as benchmark. Work on simulation of the C64 DSP was begun.

1.3.9.1.2 Prototype

Milestone	Baseline	Previous	Forecast	Status
Decision Taken on Processor Hardware	10-Dec-01	--	10-Dec-01	On Schedule

1.3.10 Forward Calorimeter

1.3.10.1 FCAL1 Module

1.3.10.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
FCAL1-C Interconnects Complete	30-Apr-01	--	30-Sep-01	Delayed (See #1)
FCAL1-C Tube Swaging Complete	1-Oct-01	--	31-Aug-01	On Schedule (See #2)
Delivery 1st half - FCAL1-A	3-Dec-01	--	3-Dec-01	On Schedule (See #3)
FCAL1-A Matrix Plate Inspection-1	10-Dec-01	--	10-Dec-01	On Schedule (See #4)

Note #1 The order for the interconnect boards has been placed.

Note #2 We are ready to start tube swaging. Baring unforeseen difficulties we expect this to move along at about the schedule shown. But our Canadian colleagues are experiencing difficulties with their swage guns. Parts break periodically. We didn't have such difficulties with Module 0 but we'll see how well the swage gun stands up for a complete module.

Note #3 This refers to the matrix plates. We expect them well before the baseline date but the exact contract delivery dates are uncertain at this time due to a pending change order.

Note #4 Our inspection procedures are well established but we will have a new tech doing them. Again we expect this to be completed well before the baseline date shown here.

John Rutherfoord (University Of Arizona)

FCal1 Module

On Friday 27 July the last tube (of 12260) was inspected and inserted into the FCal1C matrix. None had any trouble passing all 18 matrix plates. This means that the tolerance on the location and size of the holes in the matrix plates was adequately large, or perhaps too sloppy. We would have preferred a tighter tolerance and at least a few tight fits. We are now ready to swage the signal ends of the tubes into the specially designed swaging grooves to make good electrical contact for the ground return. In the meantime the rod cleaning is now up to speed and we have cleaned about 6000 so far. These rods come from the collection of about 15000 rods (out of about 26000 total, including spares) which have had holes for the signal pins drilled into one end.

We have hired a new engineering aide, Peter Truncale, former Brookhaven contract worker in cryo, to replace Ted Moreno. Peter's first day of work was July 31st. He will play a major role in the module production, particularly the A end, when others are at CERN seeing to the final assembly of the C end.

The proposed change of the FCalA modules from identical to mirror symmetric (see last month's progress report) was described in the LArG Full Meeting, reviewed by the LArG leadership, and considered by the Steering Group. Daniel Fournier made the point that such a change just substitutes one symmetry for another we already have. There were no other objections to such a change and some support for it so Horst deemed the decision to be made in our favor. We have communicated the change to the STC, the machine shop working on the matrix plates now for the A end. There will be an additional cost we estimate at about $12k (and some potential delay) due to this change. While scheduling of the A end is tight, this potential delay is not a concern.

About the same time the STC pointed out to us that a few of the raw matrix plates were warped a bit out of tolerance. This probably came about during one of the many unanticipated movements of the stored matrix plates during the extended time we were waiting for Project Office approval for the selected machine shop bid. Luckily we ordered two spare plates (in addition to the 36 plates required). So the proposed solution is to face all the FCal1A plates to a smaller (but uniform) thickness and add an additional absorber plate for a total of 19 plates at the same total depth (in z). But this requires the STC to machine an additional plate requiring more labor and time. We are working with the STC to write a change order for both this change and the mirror symmetry change at the same time. We estimate about $18k on top of the $12k noted above. No time estimate is available yet but, again, a delay is not a concern because of our flexibility in choosing the order in which we process the matrix plates.

Other than these changes and the confusion generated during the decision making process, the STC is making good progress on the A matrix plates. The shop foreman with whom we dealt during all the contract negotiations has retired and the machinist who is doing our plates has stepped up to fill his shoes. So far it appears to be a smooth transition. Leif Shaver visits the shop between LArG Weeks to monitor progress and to discuss problems.

Leif Shaver visited SIMIC in Italy the last week of June. SIMIC is the company producing the endcap calorimeters and, of particular interest to us, the aluminum support tube into which our FCal modules will be inserted during the final assembly phase. Leif took with him some precision measuring tools and one of our PVC models of a matrix plate. He found that the inner bore of this support tube was machined well enough to fit our modules as planned. Also the inner cold tube which surrounds the beam tube also fits. However it was discovered that the cryostat group has changed the order in which the bellows will be attached to the rear bulkhead, thus requiring us to make a small modification to our final assembly sequence. We will no longer be able to mount the rear bulkhead on our mandrel before bringing the support tube over our modules. We are now concerned how we will be able to mate the support tube to the rear bulkhead with the tube distorted by the weight of the FCal modules inside. Perhaps some clever temporary support for the assembly will accommodate this maneuver.

Leif is presently visiting our Australian colleagues who are responsible for the ‘plugs’ that go in the rear of the end cap cryostats. Of particular concern to us are plugs 2 and 3 which surround our support tube and go inside our support tube, respectively. Armed with detailed measurements of the support tube for the C end Leif will check that these plugs will fit.

Bids for the interconnect printed circuit boards, which hold the sockets which attach to the signal and ground pins on the module, were received and the order placed. We had hoped that the same company that will produce the boards would also stuff them but that part of their quote was too high. So we will go for separate bids on the stuffing.

1.3.10.2 FCAL Electronics

1.3.10.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
PCBs received at AZ	21-Nov-00	--	15-Dec-01	Delayed (See #1)
A Cables Delivery from Axon	2-Jul-01	--	2-Jul-01	Completed (See #2)

Note #1 Bids are out. We expect responses in early August.

Note #2 Delivery was early July, essentially on schedule. Acceptance tests are in progress.

John Rutherfoord (University Of Arizona)

Cold Electronics:

The remainder (second half of the total order) of the Axon cold cable harnesses were delivered in early July, right on schedule. We are now acceptance testing these, with statistical sampling, including physical measurements of length and a cycle of warm, cold, warm measurements of current draw at high voltage, 600 V in our case.

The acceptance testing delayed our progress on the completion of the cable characterization station. The relay boards are ready for testing and the controller board still is not completely programmed.

The summing boards are out for quote. While we are waiting for responses we are still making minor modifications to the layout. Most of the blocking capacitors (a very long lead time item) have arrived and some of the protection resistors are here. The first evaluation sample of 100 transmission line transformers is expected in early August. We plan to irradiate about 50 of these at Dubna this Fall to test for argon poisoning. As soon as we evaluate these samples we will place the final order for 4000 transformers.

1.4 TILE

Milestones with changed forecast dates:

1.4.3.3.3 Production

Milestone	Baseline	Previous	Forecast	Status
MB Card Test 10% Complete	1-Mar-01	31-Jul-01	1-Oct-01	Delayed (See #1)

Note #1 On track for current forecast and not on critical path.

1.4.1 Extended Barrel Mechanics — James Proudfoot (Argonne National Lab.)

Construction of submodules and modules continues to hold to the planned schedule. Submodule production at the University of Chicago is complete. Repair of one of the 4 UC submodules which failed to meet the design height has been completed. One of the 5 UC submodules with deformed slots is in the process of being unstacked. 169 submodules have been completed at Argonne and 152 completed at the University of Illinois and shipped to Argonne.

38 modules have been constructed, of which 32 have been fully instrumented and tested. They continue to fully meet both mechanical and optical specifications. In addition, a further 2 modules are in the final stages of testing and will be completed early in August. Module shipments to Michigan State University have been accelerated slightly to allow the institution to take advantage of additional student labor which is available in the summer months and that location is approximately one module ahead of schedule.

28 modules have been shipped to CERN. This is still 2 below the target. However, the plan is to ship 4 modules to CERN in the month of August.

Engineering design and analysis has focused on the support saddles. The design and associated report of the structural calculations is largely complete for the Extended barrel saddles. This, and the simple extension of this work to the barrel saddles and the cryostat support plates, is to be completed by the beginning of September. This work will be reviewed by the TileCal engineering group in September in order that the procurement of the first saddles may be placed in October to meet the pre-assembly schedule.

1.4.1.1 Submodules

1.4.1.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
Submodule Completion (509 Cum)	14-Dec-01	--	14-Dec-01	On Schedule

Victor Guarino (Argonne National Lab.)

During the month of July 8 submodules were constructed. The usual maintenance was performed on the production equipment and no problems were encountered during production.

Work started on dismantling the UC submodules which has closed up slots. The weld bars were ground off and plans have been made to separate the plates, Timesaver them again to remove the epoxy, and then restack them in the coming month.

Steven Errede (University Illinois-Urbana-Champaign)

In July 2001, we made 11 ATLAS TileCal submodules. We have now made a total of 164 submodules. Because a significant portion of the floor of our high-bay lab area here at UI is currently being replaced (wood to concrete), we shipped 8 fully-completed submodules to Argonne in mid-July. A total of 152 submodules have now been shipped to Argonne from UIUC. This floor work has now been completed and we now have full access to our building again!

1.4.1.2 Extended Barrel Module

1.4.1.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
Last Delivery of Girders	21-Dec-01	--	21-Dec-01	On Schedule

Victor Guarino (Argonne National Lab.)

During the month of July modules #37,38 and 39 were constructed. No problems were encountered during construction. Four modules were also shipped to CERN and 2 modules were exchanged with MSU.

Work continued on the analysis of the support saddle structures. Analysis concentrated this month on the seismic load case. The application of seismic loads presents a particular problem for the back cryostat support because it does not have any significant stiffness in the Z direction. In order to overcome this problem, stiffening beam has been added to the cryostat support. A complete summary of the analysis can be found at http://gate.hep.anl.gov/vjg/

1.4.1.4 Testing

Milestone	Baseline	Previous	Forecast	Status
Beam test Series A	2-Oct-01	--	2-Oct-01	On Schedule
Modules Source Tested (40 Cum)	31-Dec-01	--	31-Dec-01	On Schedule

1.4.2 Extended Barrel Optics

1.4.2.1 Extended Barrel Scintillator

1.4.2.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
100% Tile Deliveries from Russia Compl	2-Jul-01	--	2-Sep-01	Delayed (See #1)

Note #1 Tile production is completed in Russia. The sorting of tiles at CERN into lots for the 4 instrumentation sites has added a delay into the expected delivery schedule. This will not affect the module instrumentation schedule.

David G. Underwood (Argonne National Lab.)

At ANL we installed tiles in module ANL-33. Module uniformity turned out to be very good, perhaps because the tiles all came from recent batches, with no mixing.

Robert Miller (Michigan State University)

Optical Instrumentation Summary

Instrumentation of the US Tilecal extended barrel modules continued on schedule in July. Two modules were completed at MSU and one was completed at ANL. A total of 34 modules have been instrumented and tested, with 4 additional modules in various stages of production.

At MSU, modules ANL-31 and 34 were completed in July and scanned with the LED source. Module 34 was shipped back to ANL and 31 were ready to ship. Module ANL-37 was received at MSU and prepared for instrumentation. Tiles were inserted in ANL-35 and 37. Fibers were inserted, routed, glued and polished in Module 35.

1.4.2.2 Extended Barrel Fibers

1.4.2.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
65% Fibers in Profiles from Lisbon to ANL & MSU	2-Jan-01	--	1-Jul-01	Completed

David G. Underwood (Argonne National Lab.)

At Argonne, fibers were installed in module ANL-33. There were problems with 5 fibers, and the problems are similar to those in recent modules. The problems seem to come from damage to the fibers by the profile-stuffing machine. All the problems are in B fibers of size 72. The damage is near the end of the fiber within the aspirin tube. A scan of fibers with the camera before gluing caught a few of these, but 5 were not caught and had to be replaced after gluing.

1.4.2.3 Optical Installation Fixtures

1.4.2.3.3 Production

David G. Underwood (Argonne National Lab.)

The LED bar used to check fiber routing developed several short circuits. These were easily repaired.

1.4.2.4 Supplies

1.4.2.4.3 Production **David G. Underwood (Argonne National Lab.)**

Generally supplies of tiles, profiles, laser fibers, etc are adequate with just in time delivery of the profiles. There was some concern when a shipment of profiles took a month to arrive and be cleared through customs in Chicago because MSU needs profiles at a higher rate during the summer.

Robert Miller (Michigan State University)

The module instrumentation rate at MSU during July was accelerated due to the full time availability of the student workers. We have reached the limit defined by the production of modules and other components.

1.4.3 Readout

1.4.3.1 PMT Block

1.4.3.1.3 Production **Steven Errede (University Illinois-Urbana-Champaign)**

We completed STEP1 testing of Batch 5 PMTs during July 2001. Only one PMT from this batch failed Step1 criteria. We spent time working on getting Step2 working/running. At the end of the month, batch 6 PMTs arrived.

1.4.3.2 Front-end 3-in-1 Card

1.4.3.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
3-In-1 Card Test 100% Complete	30-Nov-01	--	30-Nov-01	On Schedule

James Pilcher (University Of Chicago)

As reported previously, production of 3-in-1 cards by the vendor is complete and all cards have been received at Chicago for burn-in and testing.

In July 1386 3-in-1 cards passed burn-in and testing and were shipped to CERN. This brings the overall number shipped to 6843 or 65% of the total. The monthly average over the 8-month period since burn-in and testing began is now up at 760 cards per month and our most recent 3-month running average is 1188 per month. Our original estimates were for 867 per month. Thus our current throughput is above the expected rate and the long-term average should continue to climb slowly.

1.4.3.3 Front-end Motherboards

1.4.3.3.3 Production

Milestone	Baseline	Previous	Forecast	Status
MB Card Fab 25% Complete	12-Feb-01	--	31-Jul-01	Completed (See #1)
MB Card Fab 50% Complete	28-Feb-01	--	31-Jul-01	Completed (See #2)
MB Card Test 10% Complete	1-Mar-01	31-Jul-01	1-Oct-01	Delayed (See #3)
MB Card Fab 100% Complete	6-Apr-01	--	31-Aug-01	Delayed (See #4)
MB Card Test 25% Complete	1-May-01	--	1-Oct-01	Delayed (See #5)
MB Card Test 50% Complete	1-Aug-01	--	30-Nov-01	Delayed (See #6)
MB Card Test 100% Complete	24-Dec-01	--	24-Dec-01	On Schedule

Note #1-6 On track for current forecast and not on critical path.

James Pilcher (University Of Chicago)

In July we received the following numbers of motherboard sections: 108 MB1, 75 MB2, 128 MB3, and 128 MB4. This brings the corresponding totals to: 143, 152, 152, 152, or as a fraction of the total order we have received 53%, 56%, 56%, 56%. We expect delivery of the motherboard sections to be complete next month.

The final part of the motherboard system is the small Mezzanine Card used for control purposes. The start of its production was delayed because of the delay in obtaining the CERN TTCrx ASIC. At this point the pre-production is complete and full production approved, all parts have been checked in at the assembly firm and the bare boards are being fabricated. Volume deliveries should begin in early September. A total of 16 sets are on hand from the pre-production process.

A total of 15 sets of compete motherboard systems have been burned in, tested and delivered to CERN. These have been used to equip the electronics drawers for the production calorimeter modules being calibrated in the test beam in August and September.

1.4.3.6 Read System Management

Milestone	Baseline	Previous	Forecast	Status
Test BM Calib of 4 Prod. Modls.	1-Oct-01	--	1-Oct-01	On Schedule

James Pilcher (University Of Chicago)

TileCal is on schedule to do test beam calibration of 2 production barrel modules and 4 production extended barrel modules this summer. Materials for the electronics drawers have been provided to Clermont Ferrand for their integration work. This includes 3-in-1 cards, Mother Board systems, and

Interface Cards. The latter have, so far, been provided by Chicago off the project budget. There is no hang-up from lack of US items.

1.4.4 Intermediate Tile Calorimeter

1.4.4.1 Gap Submodules

1.4.4.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
Scintillator procurement	1-Oct-00	--	1-Oct-01	Delayed (See #1)
Start Scintillator Assembly	1-Dec-00	--	1-Nov-01	Delayed (See #2)
Ship submodules 37-40 to ANL	11-Jun-01	--	11-Aug-01	Delayed (See #3)
Ship submodules 41-44 to ANL	27-Aug-01	--	27-Aug-01	On Schedule
Ship submodules 41-44 to BCN	3-Sep-01	--	3-Sep-01	On Schedule
Ship submodules 45-48 to ANL	26-Nov-01	--	26-Nov-01	On Schedule
Ship submodules 45-48 to BCN	17-Dec-01	--	17-Dec-01	On Schedule

Note #1 Prototypes of the ITC extension scintillators were tested at the CERN test beam last summer. Based on the test beam experience, we have made final modifications to the scintillator design. Procurement will follow as soon as final drawings are approved, and funding to buy extension scintillators is available at MSU.

Note #2 Prototypes of the ITC extension scintillators were tested at the CERN test beam last summer. Based on the test beam experience, we have made final modifications to the scintillator design. Assembly will follow as soon as funding to buy extension scintillators are available at MSU.

Note #3 Due to delayed startup of production in 1999, we are 2 months behind original schedule. There is no impact on module production.

Kaushik De (University Of Texas At Arlington)

Two ITC submodules were shipped on schedule to Argonne. Two submodules were also shipped to Barcelona. A third one was packed and held back on request from Barcelona - due to the holidays in Spain. It will be shipped together with the next shipment scheduled at the end of August.

Special ITC submodule production is proceeding smoothly. We are also recovering bad plates at a steady pace. We have built up enough extras that we will shut down stacking during the first two weeks in August, while our supervising technician, Victor Reece, is at CERN installing ITC covers on instrumented modules.

We received our second batch of 250 PMTs and have started testing them. We have still not received the hardware needed for Step II testing.

1.4.4.2 Cryostat Scintillators

1.4.4.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
Scintillator procurement	1-Dec-00	--	1-Dec-01	Delayed (See #1)
Start Scintillator Assembly	7-Sep-01	--	7-Sep-01	On Schedule
Management Contingency Go-Ahead	1-Oct-01	--	1-Oct-01	On Schedule

Note #1 Scintillator purchase and production of the ITC crack scintillators is delayed pending the decision to authorize this part of the project that was included in the management contingency fund. That decision is scheduled for 1 Oct. 01. Funding for the mechanical components was approved in Feb. 01, and those components will be purchased in FY 01.

Robert Miller (Michigan State University)

Production of the ITC fiber assemblies continued during July. The final set of standard assemblies were prepared for Barcelona. Work also continued on the special assemblies required for modules with the modified ITC submodules.

1.5 MUON

Milestones with changed forecast dates:

1.5.7.3.11 BMC Chamber Assembly Station

Milestone	Baseline	Previous	Forecast	Status
Start EIS1 Production	10-Jul-01	10-Jul-01	17-Jul-01	Completed

1.5.11.4.2 Sparsifier Prototype

Milestone	Baseline	Previous	Forecast	Status
Sparsifier 1st Proto in Hand	1-Aug-01	15-Jul-01	15-Aug-01	Delayed (See #1)

Note #1 Generic processing unit prototype complete and tested. Motherboard layout took longer than expected, but was completed in July. Motherboard printed circuit boards were ordered 31-Jul-01.

1.5.11.5.2 ROD Prototype

Milestone	Baseline	Previous	Forecast	Status
RODs 1st Proto in Hand	2-Apr-01	15-Jul-01	15-Aug-01	Delayed (See #1)

Note #1 Generic processing unit prototype complete and tested. Motherboard layout took longer than expected, but was completed in July. Motherboard printed circuit boards were ordered 31-Jul-01.

1.5.11.7.1 Software design

Milestone	Baseline	Previous	Forecast	Status
S/W Conceptual Design Review	2-May-01	15-Jul-01	1-Oct-01	Delayed (See #1)

Note #1 Development of code external to ROD and documentation not ready for review.

1.5.12.4.5 EIS1 (Boston)

Milestone	Baseline	Previous	Forecast	Status
Ship to Site	16-Feb-01	1-Aug-01	1-Sep-01	Delayed (See #1)

Note #1 The first 3 kits have been shipped. Complete shipments awaiting availability of V2 header cards.

1.5.12.4.17 EMS2 (Seattle)

Milestone	Baseline	Previous	Forecast	Status
Ship to Site	23-Jan-01	1-Aug-01	1-Sep-01	Delayed (See #1)

Note #1 The first 3 kits have been shipped. Complete shipments awaiting availability of V2 header cards.

1.5.4 CSC Chambers

1.5.4.4 CSC Construction

Milestone	Baseline	Previous	Forecast	Status
Start CSC Chamber Production	1-Mar-01	--	1-Sep-01	Delayed (See #1)

Note #1 Start of production will likely slip further pending completion of the work on documentation, procurement specification, and other open issues identified during the November 27 PRR.

Venetios Polychronakos (BNL)

We have now satisfied all requirements and have acted on all recommendations of the Production Readiness Review (PRR) of November 27 of last year. The full set of drawings was presented at the May Muon Subsystem progress review, and the procurement documents were reviewed and approved by the ATLAS PRR office at the end of July. The CSC performance review was performed on June 2 and, although the written report is not yet available, the committee expressed their satisfaction, especially since the perceived reduced track reconstruction was due to a software error in the Saclay track reconstruction code.

Orders for all materials needed for the first 5 chambers have been issued and the last parts are expected to be shipped on 30 August, so that construction will start on schedule. Meanwhile the bid package for the remaining material is ready to be sent to the BNL contracts and procurement department.

During the June Muon Workshop at Gaeta, a potential problem with energetic neutrons (neutrons with energies >0.1 MeV) was discussed by the TGC group. Neutrons at these energies loose energy primarily via elastic scattering with the atoms of the detector gas. The average ionization energy loss in such collisions can be many times larger than that of a minimum ionizing particle. This can present a problem for both the front-end electronics and the aging properties of the detector. We decided to study this effect for all four muon technologies. A model is being developed by V. Tcherniatine and an ATLAS note is being prepared. The results will be discussed during the next muon week at the end of August.

1.5.4.4.1 CSC1

Milestone	Baseline	Previous	Forecast	Status
4 Chambers Complete	1-May-01	--	1-Dec-01	Delayed (See #1)
16 Chambers Complete	2-Oct-01	--	30-Apr-02	Delayed (See #2)

Note #1-2 This milestone follows the delay in start of construction, now scheduled for September 1.

1.5.4.5 CSC Support Structure

Milestone	Baseline	Previous	Forecast	Status
Start Support Structures Construction	3-Jan-01	--	3-Dec-01	Delayed (See #1)

Note #1 The small wheel fabrication is expected to be launched by the end of the year. The contract and follow-up will be CERN responsibility.

1.5.7 MDT Chamber Production

1.5.7.1 Enginering Management

1.5.7.1.1 Chamber Integration Drawings

Milestone	Baseline	Previous	Forecast	Status
Complete Chamber Integration Drawings	1-Jul-01	--	1-Oct-01	Delayed (See #1)
Chamber Integration Drawings	28-Sep-01	--	28-Sep-01	On Schedule
Chamber Integration Drawings	28-Sep-01	--	28-Sep-01	On Schedule

Note #1 The complete chamber assembly drawings for the EIS1, EMS4 and EMS2 were delayed until the FC configuration for these chambers was finalized. This occurred during this reporting period and completion of these drawings is in process. Information on T-sensor, B-Sensor and survey target locations remains top be defined. The drawings will be updated with this information as it is released.

Richard Coco (MIT)

During this reporting period the top-level chamber assembly integration drawing for the BMC Series 2 chamber EIS1 was initiated. Once this drawing has been completed, the documentation effort will focus on the Series 2 U Michigan chamber EMS4; and next the U Washington Series 2 chamber EMS2.

The multi-layer drawings for the EIS1, EMS4 and EMS2 chambers were completed during an earlier reporting period and distributed to each of the three production sites.

T-Sensor locations were defined by U Washington (P.Mockett) and will be included as part of the top-level chamber assembly drawings. B-Sensor and alignment target locations will also be included once the final location of these sensors is defined.

1.5.7.1.2 Engineering Documentation — Richard Coco (MIT)

Engineering documentation for the final of the four Faraday cage configurations was completed. This for the 4x6x8.5 Degree chambers EIS1, EIS2. Drawings were released for pre-production run by the sheet metal vendor - Bay State Metal Products.

Machining drawings for all gas bar configurations were completed, signed-off and released to the U Washington Machine Shop for manufacture.

Engineering documentation is now focused on completing the top-level chamber assembly drawings for the Series 2 chambers EIS1, EMS4 and EMS2.

1.5.7.1.4 QA/QC Engineering Support — Richard Coco (MIT)

Engineering QA/QC activities include chamber production drawing review drawing and support to the chamber building efforts as requested.

QA/QC of the pre-production FC parts for the 3x8x14 Deg chamber at U Washington was supported by engineering. D. Marzocchi traveled to U Washington to fit the FC parts on one of the EML2 chambers completed at that site. Several minor manufacturing errors were found which were reported to the FC vendor Bay State Metal Products for correction prior to the production run.

1.5.7.1.5 Project Engineering — Richard Coco (MIT)

Project engineering responsibilities include supervision of the chamber design and documentation activities based at BMC, maintaining the chamber production schedules for chamber build at the three sites and other chamber build supporting activities as requested by the project office.

1.5.7.2 Design of Chambers and Tooling

1.5.7.2.1 Faraday Cages

Milestone	Baseline	Previous	Forecast	Status
Finished Faraday Cage Designs	21-Dec-00	--	22-Aug-01	Delayed (See #1)

Note #1 FC for EIL1 is complete and parts have been made. Designs of FC for the 3x8x8.5, 3x8x14 and 4x6x 8.5 Deg chambers have been completed and released for pre-production run. These will be evaluated for fit on production chambers, the design tweaked if necessary and released for production. The remaining FC design activities are: (1) Design an HV electrical feed interface and (2) Design the electronic shielding box for the 4x6 and 3x8 Mezzanine cards. Both these activities are delayed as the electrical group finalizes the PWB designs.

Richard Coco (MIT)

Drawings for all four Faraday cage configurations have been completed. These include 4x6x14DeEg, 4x6x8.5Deg, 3x8x14 Deg and 3x8x8.5 Deg chambers.

The remaining parts of the Faraday cage which still require design effort are the mezzanine card boxes and the HV power feed box. These designs will be completed once the final configuration of the electronic cards is defined.

1.5.7.2.2 Gas System

Milestone	Baseline	Previous	Forecast	Status
Finish Gas System Design	7-Jun-01	--	15-Aug-01	Delayed (See #1)

Note #1 Design efforts now focus on design of the gas system for the special chambers with cutouts. Design of EIL2/3/special gas bar is in process. The gas system design efforts are also focused on the layout of the gas feed tubing which carries the gas from the inlet block to each gas manifold bar.

Krzysztof Sliwa (Tufts University)

On July 13th Tufts completed fabrication of all 500 (plus a few spares) NORYL gas blocks and delivered the pieces to Harvard shop.

Richard Coco (MIT)

The design of all components of the gas supply system on each chamber have been completed except for the 6 mm gas feed line which runs from the inlet gas block to the gas manifold bar. Design of this gas feed line for EIL1 chamber has been completed and are in process for the other chambers.

Gas manifold machining drawings were released for manufacture.

1.5.7.2.4 Chamber Analysis

Milestone	Baseline	Previous	Forecast	Status
Finish FEA Modeling	30-Aug-01	--	30-Aug-01	On Schedule

1.5.7.2.5 design of Special Chamber Tooling

Milestone	Baseline	Previous	Forecast	Status
Finish all Special Chamber Tooling	27-Sep-01	--	27-Sep-01	Delayed (See #1)

Note #1 Completion of this task will probably be delayed but will be ahead of need.

Richard Coco (MIT)

Conceptual design studies for providing cutouts in the EMS1 and EMS3 chambers for alignment line clearances have been initiated. The approach under study is to provide the clearance by introducing a 130-140 mm cutout within the tube multilayers around which electrical and gas connections will be routed. A special design faraday cage will be required to enclose the volume while providing the required clearance. A 100-mm diameter clearance volume thru each multi-layer is required by the alignment bar.

1.5.7.3 Tooling

1.5.7.3.1 Module 0-Precision Tooling

1.5.7.3.3 Series Production Precision Tooling

Milestone	Baseline	Previous	Forecast	Status
Finish Series Production Tooling	1-Feb-01	--	15-Jan-02	Delayed (See #1)

Note #1 All the Series 2 production tooling for the three U.S. MDT sites is now complete. However, parts for the special chamber tooling (Series 3 @ Seattle is the first case) are delayed because the details of the special chamber design are not yet complete. Several specifications have to be finalized - such as the location of the alignment line cutouts - before the production tooling for all the U.S. MDT chambers can be finished.

1.5.7.3.5 BMC Tube Assembly Station — Frank Taylor (MIT)

A total of 7331 tubes have been made at the BMC tube station out of which 2333 tubes for the second BMC chamber series EIS1. Operations continued being routine although there has been some difficulties with the batch leak testing and dark current certification. The dark current device has been fixed by Brandeis and spare parts were ordered for the tube swagging station in order to minimize downtime if that station should break down. Brandeis, Tufts, Harvard, MIT collaborate on the BMC station.

1.5.7.3.8 BMC Tube Test Station — Frank Taylor (MIT)

EIS1 tubes are being made and tested. See remarks on tube assembly station.

1.5.7.3.11 BMC Chamber Assembly Station

Milestone	Baseline	Previous	Forecast	Status

Start EIS1 Production	10-Jul-01	10-Jul-01	17-Jul-01	Completed

Krzysztof Sliwa (Tufts University)

Tufts continued to machine assorted components for the alignment system, under the direction of Hermann Wellenstein of Brandeis. During the second week of the month, Tufts requested clarifications of drawings for the requested components. After the clarifications were provided by the Brandeis group, machining of the requested pieces got underway at the end of the month.

1.5.7.3.14 BMC Chamber Test Station **Alex Marin (Boston University)**

Steve Ahlen reached a new limit for the BMC Mod 0 resolution: 68 microns. Please look at http://www.hepl.harvard.edu/~marin. Under the cosmic-ray results. This excellent result is better precision than the requirements.

1.5.7.6 Common Procurement

1.5.7.6.1 Procurement of Tubes **Tom Fries (Harvard University)**

The first 3 series tubes have been received at each of the US assembly sites.

1.5.7.6.2 Procurement of Wire **Tom Fries (Harvard University)**

No additional wire was received in July.

1.5.7.6.3 Procurement of Endplugs **Tom Fries (Harvard University)**

10,924 MPI-type Endplugs were received at BMC. Initial QC evaluation resulted in some concern that the parts may not meet specification. The sampled parts were returned to a well-equipped, independent inspection-engineering group familiar with the part. If their evaluation demonstrates that the parts are acceptable, the parts will be distributed to the US sites for use. These parts will provide a 6-week buffer inventory.

1.5.7.6.4 Procurement of Faraday Cage **Tom Fries (Harvard University)**

EMS & EML prototype FC parts were delivered to UM & UW respectively. UW approved the design and the order for 16 EML-2 chambers was released for delivery in August. We are awaiting completion of a chamber at UM in order to trial fit the EMS prototype parts.

1.5.7.6.5 Procurement of Gas Supply System **Tom Fries (Harvard University)**

Tubeletts:

The European supplier (Heim) submitted a pre-production sampling of 5136 pieces to BMC for final approval.

Retainer, Tubelett:

The supplier (Walter Hugin) shipped most of the production order to BMC in the last week of July.

Gas Bars:

Finished bars were shipped from UW machine shop:

20 EMS-5 Type 2 for UM, 11 EML-2 Type 2 for UW. Also, the raw Al extrusion for the Type 3 bar production was delivered to UW.

Gas Blocks were completed at Tufts and distributed to the US sites.

Extension Fitting:

An order was placed for the full series of brass extensions with a delivery expected by the end of August.

1.5.7.6.6 Procurement of Spacer Frame + Attachment Henry Lubatti (University of Washington)

1. We completed the EML3 A01-15 spacer-supports for the Michigan in July.

2. We completed 80% of the EMS3 A02-16 and 20% of the EMS3 C02-16 spacer-supports for Seattle in July.

3. Josh Wang completed series 3 production chamber drawings after receiving information from Boston on location of various electronic box and gas block locations.

1.5.7.7 BMC Chamber Construction 104

1.5.7.7.1 EIL 1 Series (WBS 1.5.7.7.1)

Milestone	Baseline	Previous	Forecast	Status
End of EIL1 series production	14-Jun-01	--	14-Jun-01	Completed

1.5.7.7.2 EIS1 series (WBS 1.5.7.7.2) Frank Taylor (MIT)

Tubes for BMC EIS1 chambers were supplied to the chamber builders ahead of the critical path.

Alex Marin (Boston University)

EIS1 Mod 17 completed as of July 31.

1.5.7.8 WBS 1.5.7.8 Michigan Chamber Construction 104

1.5.7.8.2 EMS4 Series (WBS 1.5.7.8.2) Ed Diehl (University of Michigan)

During July we finished retooling for EMS4 production and then began EMS4 production, producing 1.5 chambers in the new series.

We have taken 5 weeks for retooling and plans to start the next chamber today. Retooling proceeded fairly smoothly, but we did have some unexpected problems. We found that the 8.5-degree angle combs had developed bows of 30 microns combs. This bowing was not present initially. The bow was removed by adding shims to push up the ends of the combs. Runout is now ~12 microns in the angle combs. The straight combs do not have any bowing. This bowing seems to be related to the material used in the combs: the angle combs are made from cast aluminum whereas the straight combs are made from drawn aluminum.

Here is a summary of the 2nd chamber series production. Tube wiring already began by mid-June and now we have made 4 chambers' worth of tubes.

We did an experiment on the effect of cleaning inside tubes with an alcohol-soaked cloth to remove debris which is sometimes seen. We wanted to see if these cleaned tube had different results with the dark current test. They performed identically to uncleaned tubes in the dark current, so we conclude that cleaning has no benefit.

The gluing procedure is proceeding quite smoothly. The new gantry has been raised for this series (to pass over OPS towers) without any unpleasant side effects. UM is in the process of changing to a new glue-mixing system using hand pumps to pump and mix glue directly from 5-gallon pails (avoiding tedious Synge refills/cleaning). The system works, but some improvements are being made to the system to ensure glue quality (i.e. mixing ratio) and system robustness. In the interim, glue mixing is done with the old syringe method.

Several improvements had been made to the OPS system (diffuser glass added to masks, gantry height raised to avoid having to ever move towers, and better clamping of OPS bases). However, the OPS system works the same as before - raw measurements repeat at the 5-10 micron level for level 1-2-3 and at the level 10-20 microns for the trophy. However, it might be pointed out that this is not actually that bad, though not as good as others seem to be able to achieve.

The new inplane system was installed with a few minor start-up problems. There was a small hole placement mismatch between the short side mask fixture and the spacer frame which was fixed by enlarging the holes on the spacer frame. The new inplane electronics worked fine, though a little software tweaking was required to get everything working.

The PMO platforms were mounted with a new positioning scheme which is simpler than for series 1. UM likes the new method, and is confidant that there will be fewer problems with PMO placement than in series 1.

We began setting up an EMS5 chamber for a cosmic ray/electronics test. Faraday cage and gas system were installed and a scintillator trigger set up. We hope to have the system fully operational by August.

After making the first EMS4 base chamber we installed the Faraday cage (FC) and gasbar. The FC installation went fairly smoothly. There was one tube clocking error on the chamber requiring a small modification of the FC plate. Screw-hole alignment is easily checked by attaching each baseplate with screws only partially tightened. In this case it is easy to re-align or fix any alignment problems. A simple yet wonderful tool was developed for installing ground pins: insulation from 14-gauge wire is used to hold the ground pin and rotated to screw the pin in. A prototype HV hedgehog card was installed fit well. A check list provided by D. Marzocchi was checked and all points passed. In particular the chamber envelope was not exceeded by the FC, but the gas bar weld exceeds the envelope by about 1 mm. This was a prototype version of the FC. Since it worked well, we have given the OK to make a bulk order. Next chamber signal caps were removed and the underlying o-rings were carefully cleaned and inspected.

After this the pre-assembled gasbars were installed on the chamber which went quite smoothly. Here is a breakdown of the time required for various tasks:

1) FC installation (1600 screws & ground pins)	20 person-hours
2) 2) Gasbar tubelet pre-assembly	7-8 person-hours
3) 3) Gas pre-assembly and leak test	2-3 person-hours
4) 4) Removal of HV caps, o-ring cleaning	4 person-hours
5) 5) Installation of pre-assembled gasbar on chamber.	2 person-hours

Gas leak check is now underway.

1.5.7.9 WBS 1.5.7.9 Seattle Chamber Construction 96

1.5.7.9.3 EMS2 Series (WBS 1.5.7.9.3) Paul Mockett (University of Washington)

1.5.7.9.2.2 Seattle Chamber Production

1) The temperature interface boards from Advanced Circuits showed up, but on a hunch MT called the company to verify they were made with G-10. In fact the entire order had been made with FR-4. The company said they could get G-10, but to date haven't been able to locate any. (Chamber Construction)

2) Updated the new Rasnik board Version 1 to Version 2 using new Files from Kevan H. (Chamber Construction). We have received several sets of Inplane CCD assemblies from Brandeis. On the first chamber one new style CCD board was plugged into an old style CCD readout board. This blew the new CCD head, and a fuse on the old style multiplexer board. Also one CCD image was very dim and was found to be related to the CCD Head.

3) Also we now have lost (non-functional) 3 LED mask illumination boards. Two for no apparent reason - they worked one evening - didn't work the next morning. And one to user error - being plugged into old mask power supply (24V).

4) Found that the 2029 CCD headboard and the 2036 CCD board do indeed record the same image. This test was performed while swapping the hardware on our module 1 chamber due to a burned out 2036. Removal of 2036 was very difficult, and could easily result in damage to CCD headboard.

5) MT has completely rewritten most of the software for the clean room, with help from some of our students. Ari Lumbantobing created the framework for the Database storage routines. These allow me to save values to a database with safeguards against overwriting - MT wrote new cases for different situations like glue and no glue cases, layers, PMO, inplane measurements. Matt Stockbridge has modified a tube-scanning program for our use in scanning tubes. And Dan Allred modified and rewrote portions of my tube height program so that now 2 people can simultaneously take tube height measurements. While the values are written to the database, they will continue to be written to the harddrive along with the actual CCD images as well.

6) Rewrote the Bridgeview software for the CAN temperature controller to include the local humidity. MT found that he didn't need to reprogram CAN controller since the program it contained already was setup to read 48 channels. The channels on the board had just been tied to ground. By cutting the trace on one set of 16 channels, the humidity sensor was connected along with all 16 T sensors. The software now has a feature that once OPS for a layer, the I-inplane measurements, or the trophy height pictures have been taken, an average RO and HV side temperature is taken, along with the humidity, and stored into the Database, as well as a text file. The program by default takes a temperature reading every 5 minutes. Also the program now creates a new file at midnight - thus each day's temperatures has it's own file.

7) Made 4 new long distance cables for the inplane measurement system with Denise Dennis. This required Hilift to string cables overhead on gantry system. These lines will be dedicated to the new Hardware to prevent any more burnouts. Instructed Denise in crimping techniques for RJ-45 cables.

8) We are finding that the temperature in our clean room is not very stable. There are odd increases in temperature which need to be fixed. The new data logging of temperature has made it far easier to notice the change in temperature since there is now only one day's worth of temperatures in a file. Kirby and Jason have both been alerted to the problem.

9) 64 Meg memory added to the clean room 233MHz computer for a total of 128MB

10) MT doesn't want to upgrade the system downstairs until we can swap in a new system. Since we are actively using it for construction, MT doesn't want to mess with it too much. Did find and replace one burned out fan in it already.

11) Set up the new hardware in the hi-bay area for checking the inplane system during spacer frame assembly.

12) We have received 1700 of ~4900 TMP37 temp sensors from Newark. More will arrive soon.

13) Concluded changeover from EML2 to EMS2 fixturing which included: Installation of tube ht. measuring shelves, placement of Peemo bases and calibration of tube ht. in combs and profiles of 8.5 deg. combs with shelves installed. Test runs of gluegun and optics and sorting out software for measuring barcodes, OPS and tube heights. Modified multilayer spreader bar for lifting ML1 of each chamber back into combs. Modification of spacer frame gluing locator when assembling chamber.

14) Finished construction of EMS2.A02 spacer frame by fitting it with the inplane Rasnik system.

15) Begin construction of EMS2 chambers on 7/18/01.

16) Completed EMS2.A02, Chamber 1, except for gas and electronics services.

17) Begin construction of EMS.A04, Chamber 2. Finished its ML1 on 7/31/01.

Henry Lubatti (University of Washington)

We produced and tested 878 EMS2 tubes in July.

1.5.8 MDT Supports

1.5.8.1 Mechanical design

1.5.8.1.2 Chamber Mount Struts Henry Lubatti (University of Washington)

Josh Wang generated working drawings of the concept developed in Italy for adjustable connections to the wheel mount plate and submitted drawings to shop for quotes.

1.5.8.1.3 Integ with Support Structure

Milestone	Baseline	Previous	Forecast	Status
(SM Wheel) CERN Design/FEA Complete	15-Jul-00	--	1-Dec-01	Delayed (See #1)
(Big Wheel) CERN Design/FEA Complete	1-Feb-01	--	15-Dec-01	Delayed (See #2)
50% Complete	1-Aug-01	--	1-Aug-01	On Schedule

Note #1 A large fraction of this work has been completed, but as we depend on CERN for the detailed small wheel design from CERN and others for alignment bar and plumbing information we have a delay. Some small progress was made in July. We forecast that this will not be completed until December 1, 2001.

Note #2 Because we depend on CERN for the detailed big wheel design and others for alignment bar and plumbing information we have a delay. We forecast that this will not be completed until March 15, 2002. The May design report on the Big Wheel showed much progress but the final drawings and bid specs will not likely be available until December 15, 2001. It is expected that there will be further design and installation changes during the bid process.

1.5.8.2 Production

1.5.8.2.1 Kinematic Mount Production

Henry Lubatti (University of Washington)

We completed 25% of the EIS2 A01-15 kinematic mounts for Michigan in July.

1.5.9 MDT Electronics

1.5.9.1 Mezzanine Card

1.5.9.1.1 MDT-ASD

Milestone	Baseline	Previous	Forecast	Status
ASD PRR	19-Oct-01	--	19-Oct-01	On Schedule

George Brandenburg (Harvard University)

Six ASD01a prototype chips have been successfully tested. All seems to be OK, except the adjustable deadtime which is shorter than expected (approximately equal to the total drift time). It is under discussion whether this presents any problems.

1.5.9.1.2 Mezz PCB

Milestone	Baseline	Previous	Forecast	Status
Mezz PCB Certified	16-Nov-01	--	16-Nov-01	On Schedule

George Brandenburg (Harvard University)

One production prototype (410) has been completed and we are working on the layout of the second one (411).

The current plan is to have only three mezz board types for final production: one 3x8 design which works both for type I and II hedgehogs, and two 4x6 designs which work for type III and IV hedgehogs respectively. The mezz-csm cable connector would in all three cases be oriented parallel to the plane of the chamber. This way the cable can lay flat on the top surface of the FC and exit at a right angle to the spacer frame area. Sketches of these designs (board outline, connector location, mounting holes) will be circulated soon.

1.5.9.2 Hedgehog Cards

1.5.9.2.1 Signal Hedgehog 3X8

Milestone	Baseline	Previous	Forecast	Status
Hedgehog PCB Certified	30-Aug-00	--	1-Aug-01	Delayed (See #1)
Hedgehog Production Complete	28-Feb-01	--	31-Dec-02	Delayed (See #2)

Note #1 Delayed to consider design changes: shortening, coating change. Also the HV capacitor vendor selected is unacceptable to CERN; we must evaluate other vendors and choose a replacement.

Note #2 Production will most likely now take place at CERN starting in the last quarter of 2001. The first production quantities should be available at the end of 2001. Production will continue during 2002 in parallel with chamber building.

1.5.9.4 Chamber Service Module

Milestone	Baseline	Previous	Forecast	Status
CSM-1 Prototype	1-Sep-00	--	1-Jun-02	Delayed (See #1)
CSM-1/Octal ASD/MROD Test	1-Dec-01	--	1-Dec-01	On Schedule

Note #1 The scope of the CSM-1 has recently changes to a simpler, more robust design. As a result the completion date of the first prototype has moved to spring 02. Work on the design for this more ambitious design is progressing.

1.5.11 CSC Electronics

1.5.11.1 ASM1 Boards

1.5.11.1.1 Design

Milestone	Baseline	Previous	Forecast	Status
Preamp/Shaper Final Design Review	2-Oct-01	--	1-Dec-01	Delayed (See #1)
System Critical Design Review	2-Oct-01	--	1-Dec-01	Delayed (See #2)

Note #1-2 Delayed to allow us to verify design modifications to preamp/shaper for yield enhancement, reduced crosstalk, and improved overload recovery.

Anand Kandasamy (BNL)

Front-end Preamp/Shaper monolithic was redesigned during the month of June-July to address the issue of lowering the input impedance and to improved the overload recovery response of the amplifier. Also, the total number of channels/packaged IC was increased from 16 (12 signals, 4 reference) to 25(24 signals, 1 reference).

ASM I (preamp/shaper) board and ASMI to ASM I flex cable have been designed and are to be prototyped and tested.

Test Fixtures are being designed for testing the prototypes and production units of ASM Packs.

1.5.11.2 ASM II Board

1.5.11.2.1 ASM II Board design

Anand Kandasamy (BNL)

[SSJ]

1] ASMII-b board design: The preliminary design of the ASMII-b is complete and is being reviewed. This board has 16 SCAs (8 mirrored and 8 nonmirrored) and as many ADCs on it. MAX7000 (MAX7064) series FPGA is chosen for multiplexing these ADC Outputs to the serializer for G-link (16 bits input is serialized).

2] Experimented with the existing ASMII-a boards for various modes of operations for the G-Link.

3] Since ASMII-b has an APEX Chip on it, it was concluded that its good to have a flexibility of operating the G-Link in the Simplex or full Duplex mode, instead of hard wiring the G-Link Daughter boards for the Full Duplex mode.

4] The design by Anand for the HP-Version of the mulitplexar chip was simulated using MAX+Plus II and the same design will be downloaded on the MAX chips on the ASMII-b boards. HP Chip and this ALTERA FPGA have the same pin assignments.

[AK]

ASM2MUX was designed and submitted to MOSIS in HP 0.5-micron technology.

1.5.11.4 Sparsifiers

1.5.11.4.2 Sparsifier Prototype

Milestone	Baseline	Previous	Forecast	Status
Sparsifier 1st Proto in Hand	1-Aug-01	15-Jul-01	15-Aug-01	Delayed (See #1)

Note #1 Generic processing unit prototype complete and tested. Motherboard layout took longer than expected, but was completed in July. Motherboard printed circuit boards were ordered 31-Jul-01.

1.5.11.5 ROD's

1.5.11.5.1 ROD design — David Stoker (University of California Irvine)

During July we completed the layout of the prototype ROD motherboard. Six ROD motherboard printed circuit boards were ordered. Verilog code for the ROD PLD's was revised due to layout-induced ROD design changes. We continued developing C and assembly code for the ROD's SPU (Sparsifier Processing Unit). We also continued C coding of the Clock Generation drivers, which run in the ROD's HPU (Host Processing Unit).

1.5.11.5.2 ROD Prototype

Milestone	Baseline	Previous	Forecast	Status
RODs 1st Proto in Hand	2-Apr-01	15-Jul-01	15-Aug-01	Delayed (See #1)

Note #1 Generic processing unit prototype complete and tested. Motherboard layout took longer than expected, but was completed in July. Motherboard printed circuit boards were ordered 31-Jul-01.

1.5.11.7 Software

1.5.11.7.1 Software design

Milestone	Baseline	Previous	Forecast	Status
S/W Conceptual Design Review	2-May-01	15-Jul-01	1-Oct-01	Delayed (See #1)

Note #1 Development of code external to ROD and documentation not ready for review.

1.5.12 Global Alignment System — Jim Bensinger (Brandeis University)

Once again our principal activity this month has been working on H8. The stands for EO, EM, and EI were installed. EO and EM were surveyed, EI has yet to be installed in the proper place. Work continues preparing the phantom chambers for installation. We are also toiling away at producing the various mounts and struts for installation of mechanical components. We are laying out and producing the various boards needed for the variety of devices used in H8.

We continue to ship inplane systems and proximity mounts for the second round of production. These devices used the new Long Wire alignment DAQ (V2).

1.5.12.1 Global Design

1.5.12.1.1 Alignment Bars

Milestone	Baseline	Previous	Forecast	Status
Alignment Bar Design Complete	30-Mar-01	--	30-Mar-02	Delayed (See #1)

Note #1 Design for H8 is complete and there is no work on this item at this time. This design will be reviewed following analysis of H8 results. (By then we hope TC will stop moving the wheels around.) Final design will take place at that time.

Jim Bensinger (Brandeis University)

The drawings for the device mounts on the long bars were completed. We are still working on the mount drawings for the short bars. The long bar mounts to be made in the Brandeis shop were completed. The drawings for the ones to be made at Freiburg have been sent to Freiburg to be produced on their new 5-axis mill. Our technician went to Freiburg to help with the installation of the mounts on the bars.

The first bar (EO upper) was measured; preliminary analysis indicates that once calibrated, the prediction of deflection under load is better than our requirements. Analysis is continuing.

1.5.12.1.2 Proximity Monitors

Milestone	Baseline	Previous	Forecast	Status
Proximity Monitor Design Complete	29-Sep-00	--	7-Aug-01	Delayed (See #1)

Note #1 Delays in H8 and new information from simulation have pushed this item back.

Jim Bensinger (Brandeis University)

The mechanical design of the H8 version of the proximity camera was completed. This design allow the use of 8mm, 15mm, and 20 mm diameter lenses so that a lens can be placed anywhere along the barrel of the camera. This allows for a large range with the same basic device. The extrusion for the cameras arrived at Brandeis. Layout of the header card is progressing.

1.5.12.1.3 Multi-Point System (BCAM)

Milestone	Baseline	Previous	Forecast	Status
BCAM Design Complete	31-Dec-01	--	31-Dec-01	On Schedule

Jim Bensinger (Brandeis University)

Work was begun on the low profile BCAM. There are some locations were the standard BCAM will not fit in the allowed space. This is generally a lower priority effort.

1.5.12.1.4 System Design

Jim Bensinger (Brandeis University)

Our efforts here were spent mostly detailing H8. Detailed mount drawings were done for all sensor mounts on the long bars. Detailed layouts of sensor positions for the long H8 alignment bars was completed. This is used for bar assembly and to compare to measurements on the Freiburg CMM. We responded to requests for information from the CERN muon integration group concerning the big wheel (about one week of effort).

1.5.12.1.5 DAQ

Milestone	Baseline	Previous	Forecast	Status
Complete design of H8 alignment DAQ hardware.	1-Apr-01	--	1-Aug-01	Delayed (See #1)
DAQ Design Complete	28-Sep-01	--	30-Mar-02	Delayed (See #2)

Note #1 All basic designs are completed but detailing of some components is continuing.

Note #2 The H8 version basic design is complete. This design will be reevaluated following analysis of H8 data and, if needed, will be revised at that time.

Jim Bensinger (Brandeis University)

Work continues on the Long Wire Alignment DAQ. Several new circuits were designed; the BCAM header, the BCAM peripheral head, and the device multiplexer. Two new PCB were laid out; the production version of the inplane sensor header and a corrected version of the device driver.

1.5.12.2 Operational Test Stands

1.5.12.2.3 H8 DATCHA

Milestone	Baseline	Previous	Forecast	Status
H8 Operational	24-Nov-00	--	1-Sep-01	Delayed (See #1)

Note #1 The assembly of support structures and frames at CERN has been slower than expected. This is now completed but the area will be unavailable for mounting devices for much of July because the beam will be on. Most components are expected to arrive in August.

Jim Bensinger (Brandeis University)

This month has seen continued progress in the setup of H8. The EO frame was surveyed and adjusted. It appears to be about 30 mm forward of its intended location but this will have no effect on the alignment (or any other) test. The analysis was done of the EM survey results. The frame appears badly warped. Preliminary communication with the survey group indicates they get a similar result. The EI frame was put on the stands and preliminary survey was taken indicating the floor stands were misplaced by 100 mm. The floor pads will be moved and we will try again.

The phantom chambers (5 of 6 MDTs and 1 CSC) are in the area and being prepared for installation. We are hampered by the lack of a chamber installation plan or design, not to mention installation hardware. Fortunately the phantom chambers are somewhat more sturdy than real chambers.

The alignment DAQ system is setup and running. As hardware becomes available is tested. Phantom chamber RASNIKs have been converted to the LW-DAQ V2 system. The database is setup and taking and the control program is exercised in various configurations. Some problems have been identified and a corrected version of the device driver has been produced.

The first fully equipped 9.6-meter alignment bar has been assembled and measured in Freiburg.

1.5.12.3 Global System Production

Milestone	Baseline	Previous	Forecast	Status
Align Bar/Prox Monitors PRR	3-Jan-01	--	31-Mar-02	Delayed (See #1)
Critical System Design Review	3-Jan-01	--	31-Mar-02	Delayed (See #2)

Note #1-2 Not yet scheduled but will follow analysis of H8 results.

Jim Bensinger (Brandeis University)

The part of system production that has begun is that relating to the production of MDT chambers, the inplane system and the camera mounts and mask mounts for the proximity monitors that go on the chambers.

1.5.12.3.1 Alignment Bars

Milestone	Baseline	Previous	Forecast	Status
Bar Production 10% Complete	1-Oct-01	--	1-Jun-02	Delayed (See #1)

Note #1 This is no longer a US responsibility and will be done at Freiburg. Bar production will not begin until after analysis of H8 results.

1.5.12.3.2 Proximity Monitors

Jim Bensinger (Brandeis University)

We have begun delivering the mask and camera mounts for the second round of production to the US production sites. For the second round of production 48 camera mounts and 26 mask mounts have been delivered.

1.5.12.3.4 DAQ **Jim Bensinger (Brandeis University)**

This month we built 30 inplane sensor heads, 2 Device Drivers and 10 inplane mask heads.

1.5.12.4 MDT Inplane Monitors

1.5.12.4.1 Common Items **Jim Bensinger (Brandeis University)**

Almost all of the common parts for the approved MDT chamber production now exist at Brandeis or on produced chambers.

1.5.12.4.5 EIS1 (Boston)

Milestone	Baseline	Previous	Forecast	Status
Ship to Site	16-Feb-01	1-Aug-01	1-Sep-01	Delayed (See #1)

Note #1 The first 3 kits have been shipped. Complete shipments awaiting availability of V2 header cards.

Jim Bensinger (Brandeis University)

Three kits have been delivered to Harvard. Drivers for the V2 LW-DAQ system have been updated.

1.5.12.4.6 EIS2 (Boston)

Milestone	Baseline	Previous	Forecast	Status
Ship to Site	23-Oct-01	--	1-Feb-02	Delayed (See #1)

Note #1 Changes in MDT production schedule has moved this chamber to the third round of production. Since this is a special chamber, confirmation of the inplane design will await completion of the design of the chamber.

1.5.12.4.13 ENL3 (Michigan)

Milestone	Baseline	Previous	Forecast	Status
Ship to Site	10-Dec-01	--	10-Dec-01	On Schedule

1.5.12.4.17 EMS2 (Seattle)

Milestone	Baseline	Previous	Forecast	Status
Ship to Site	23-Jan-01	1-Aug-01	1-Sep-01	Delayed (See #1)

Note #1 The first 3 kits have been shipped. Complete shipments awaiting availability of V2 header cards.

Jim Bensinger (Brandeis University)

Three kits have been delivered to Seattle. Drivers for the V2 LW-DAQ system have been updated.

1.5.12.4.18 EMS3 (Seattle)

Milestone	Baseline	Previous	Forecast	Status
Ship to Site	7-Sep-01	--	1-Apr-02	Delayed (See #1)

Note #1 This chamber is not scheduled to be built until the third round of MDT production.

1.5.12.4.19 EMS4 (Michigan)

Jim Bensinger (Brandeis University)

Three kits were sent to Michigan but unfortunately one was lost (not just misdirected) by DHL shipping. This caused some production problems. Drivers for the V2 LW-DAQ system have been updated.

1.6 TRIGGER

Milestones with changed forecast dates:

1.6 Subsystem Manager's Summary

Milestone	Baseline	Previous	Forecast	Status
LVL2 Trigger Prototype Complete	30-Sep-01	30-Sep-01	31-Oct-01	Delayed (See #1)

Note #1 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype integration is now expected to be completed at the end of October.

1.6.1.2.4 SRB Prototype Travel

Milestone	Baseline	Previous	Forecast	Status
Prototype SRB Assy Compl	30-Sep-01	30-Sep-01	30-Nov-01	Delayed (See #1)
Calo for Integ Study Compl	30-Sep-01	30-Sep-01	31-Oct-01	Delayed (See #2)

Note #1 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype integration is now expected to be completed at the end of October.

Note #2 This prototype evaluation has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype preliminary exploitation is now expected to be completed at the end of November.

1.6.2.2 Calo Protos

Milestone	Baseline	Previous	Forecast	Status
Prototype Calo Assy Compl	30-Sep-01	30-Sep-01	31-Oct-01	Delayed (See #1)

Note #1 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype integration is now expected to be completed at the end of October.

1.6.3.1.4 SCT Design Travel

Milestone	Baseline	Previous	Forecast	Status
SCT for Integ Study Compl	30-Sep-01	30-Sep-01	30-Nov-01	Delayed (See #1)

Note #1 This prototype preliminary exploitation has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype evaluation is now expected to be completed at the end of November.

1.6.4.1.4 Arch. Design Travel

Milestone	Baseline	Previous	Forecast	Status
Prototype Project Assy Compl	30-Sep-01	30-Sep-01	31-Oct-01	Delayed (See #1)
Arch Design for Integ Study Compl	30-Sep-01	30-Sep-01	30-Nov-01	Delayed (See #2)

Note #1 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype integration is now expected to be completed at the end of October.
Note #2 This prototype evaluation has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype preliminary exploitation is now expected to be completed at the end of November.

Milestone	Baseline	Previous	Forecast	Status
LVL2 Trigger Prototype Complete	30-Sep-01	30-Sep-01	31-Oct-01	Delayed (See #1)
LVL2 Trigger Design Complete	31-Dec-01	--	31-Dec-01	On Schedule

Note #1 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype integration is now expected to be completed at the end of October

1.6.1 LVL2 SRB

1.6.1.2 SRB Protos

1.6.1.2.1 SRB Protos EDIA **Robert Blair (Argonne National Lab.)**

The design of the prototype RoI Builder is progressing. Two options are being considered for the physical layer used to implement the S-link connection into and within (between the RoIB and supervisor processors) the system. One option is to use the Odin chipset and build the S-link interface on the board to keep costs down. The other option is to implement a daughtercard that uses Gigabit ethernet and make it compatible with the current Odin based daughter cards used by Level 1. This latter option is currently favored. David Francis was very concerned that the S-link hardware may change and felt it was wiser to keep the flexibility associated with a removable daughtercard.

Bernard Pope (Michigan State University)

Abolins, Pope, Ermoline and Hauser all attended the TDAQ week at CERN. In particular, Abolins and Ermoline participated actively in the LVL1-Dataflow meeting. The status for integration of the LVL1 RODs with the Region of Interest Builder, the LVL1-LVL2 document, and the RoIB Requirements document were all discussed. The ROD working group activity was concentrated on the preparation for the ROD VMEbus interface recommendation document.

1.6.1.2.4 SRB Prototype Travel

Milestone	Baseline	Previous	Forecast	Status
Calo for Integ Study Compl	30-Sep-01	30-Sep-01	31-Oct-01	Delayed (See #1)
Prototype SRB Assy Compl	30-Sep-01	30-Sep-01	30-Nov-01	Delayed (See #2)

Note #1 This prototype evaluation has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype preliminary exploitation is now expected to be completed at the end of November.

Note #2 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype integration is now expected to be completed at the end of October.

1.6.2 LVL2 Calorimeter Trg

1.6.2.2 Calo Protos

Milestone	Baseline	Previous	Forecast	Status
Prototype Calo PDR	31-Mar-01	--	31-Jul-01	Completed (See #1)
Prototype Calo Assy Compl	30-Sep-01	30-Sep-01	31-Oct-01	Delayed (See #2)

Note #1 This PDR as several others has been delayed to conform to the initial review of the Phase 2a prototype. This aligns it with the Atlas wide milestones presented to the LHCC in March.

The workshop in July served to provide a forum whereby each part of the system was presented and discussed. This provided an opportunity for scrutiny and comment on the current design. There was no formal signoff nor any requirement that comments be documented and acted on. The review was a weak one from this point of view, but was adequate for a preliminary design review at this stage of the project.

Note #2 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype integration is now expected to be completed at the end of October

1.6.3 LVL2 SCT Trg

1.6.3.1 SCT Design

1.6.3.1.1 SCT Design EDIA — Andrew Lankford (University Of Calif. At Irvine)

Study of alternative implementations of the ROD/ROB interface continued in June. A model solution of a ROBin that can be mounted on the ROD consists of an FPGA implementing an S-link interface, SDRAM buffer memory, a DSP chip, an integrated MAC/PHY chip providing a Gigabit Ethernet output, and a small amount of glue logic (PLD, flash memory, oscillator). The possibility of a network-based Readout Subsystem (ROS) was discussed in the ROS session at the July TDAQ Week. An investigation of the system implementations of such a solution was initiated in the context of the ROS Working Group.

As a follow-on to the discussions with the LArg community concerning Readout Link interface and implementations, a ROL Task Force was established in the context of the ATLAS ROD Working Group. The charge to the task force is to recommend the protocol and physical layer of the ATLAS Readout Link. Andy Lankford is a member of this task force from the TDAQ project. An interface via a connector with electrical and protocol specifications is preferred by the task force for reasons of flexibility and upgradeability; however, it must be established that such an arrangement can be accommodated by the RODs of all detector systems.

Saul Gonzalez (University Of Wisconsin)

1.6.3.1.4 SCT Design Travel

Milestone	Baseline	Previous	Forecast	Status
SCT for Integ Study Compl	30-Sep-01	30-Sep-01	30-Nov-01	Delayed (See #1)

Note #1 This prototype preliminary exploitation has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype evaluation is now expected to be completed at the end of November.

1.6.3.2 SCT Protos

Milestone	Baseline	Previous	Forecast	Status
Prototype SCT PDR	31-Mar-01	--	31-Jul-01	Completed (See #1)
Prototype SCT Assy Compl	30-Sep-01	--	30-Sep-01	On Schedule

Note #1 This PDR, as several others, was delayed to conform to the initial review of the Phase 2a prototype. This aligns it with the Atlas-wide milestones presented to the LHCC in March.

The TDAQ workshop in July served to provide a forum whereby each part of the system was presented and discussed. This provided an opportunity for scrutiny and comment on the current design. There was no formal signoff nor any requirement that comments be documented and acted on. The review was a weak one from this point of view, but was adequate for a preliminary design review at this stage of the project.

1.6.4 Architecture & LVL2 Global Trigger

1.6.4.1 Arch. Design

Milestone	Baseline	Previous	Forecast	Status
Prototype Project PDR	31-Mar-01	--	31-Jul-01	Completed (See #1)

Note #1 This PDR as several others has been delayed to conform to the initial review of the Phase 2a prototype. This aligns it with the ATLAS-wide milestones presented to the LHCC in March.

The workshop in July served to provide a forum whereby each part of the system was presented and discussed. This provided an opportunity for scrutiny and comment on the current design. There was no formal signoff nor any requirement that comments be documented and acted on. The review was a weak one from this point of view, but was adequate for a preliminary design review at this stage of the project.

1.6.4.1.1 Arch. Design EDIA **Andrew Lankford (University Of Calif. At Irvine)**

The TDAQ Project reported to the LHCC Comprehensive Review in early July, including reports on progress in the HLT/DAQ system, where U.S. involvement is concentrated. The referees concluded that there are no immediate critical issues and that the TDAQ schedule is reasonable but tight. The integrated prototyping program, particularly its Phase 2A, was seen as an important step towards choosing a single system design. Choice of a single ROBin implementation and demonstration that the offline framework Athena can be used in the Event Filter were given as illustrations of key hardware and software progress that is needed.

During the July TDAQ Week, a one-day review was held of the status of the design of the prototype system to be used in Phase 2A. Although there was no formal signoff or follow-up procedure, this session provided an opportunity to scrutinize and comment on the prototype design of each subsystem and component prior to full design and implementation for the prototype system.

Dependencies between TDAQ and offline computing development and design have been identified, and these were discussed with the Computing Coordinator. Progress on these issues will be coordinated by a set of TDAQ contacts who will participate in the Computing coordination groups (steering, reconstruction, simulation, databases).

Robert Blair (Argonne National Lab.)

A new version of the TTCpr was produced and delivered to CERN for use in the testbeam and in future testbed setups. Integration in the testbeam was done by Jim Schlereth during the second week in July. This version uses the latest TTC receiver ball grid array.

Bernard Pope (Michigan State University)

Abolins had discussions with the ATLAS Trigger/DAQ leader, Andy Lankford, on the LVL2/DAQ-EF integration. He also discussed the Speaker Committee document with other committee members (Klaus Pretzl, Karl Jakobs) and Leandro Nisati, chair of the T/DAQ IB. Pope participated in meetings of the PESA (Physics and Event Selection Algorithm) subgroup. Hauser organized the DataCollection session and gave various talks.

Further comments on the message passing were received from the ROS group, and changes were incorporated in the relevant documents. A first version of the message passing based on UDP was implemented and made available in cvs.

1.6.4.1.4 Arch. Design Travel

Milestone	Baseline	Previous	Forecast	Status
Arch Design for Integ Study Compl	30-Sep-01	30-Sep-01	30-Nov-01	Delayed (See #1)
Prototype Project Assy Compl	30-Sep-01	30-Sep-01	31-Oct-01	Delayed (See #2)

Note #1 This prototype evaluation has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype preliminary exploitation is now expected to be completed at the end of November.

Note #2 This prototype completion has been delayed to be consistent with the current ATLAS TDAQ schedule. The Phase 2A prototype integration is now expected to be completed at the end of October.

1.6.4.2 Global Production

1.6.4.2.1 Global Prod Eqmt **Saul Gonzalez (University Of Wisconsin)**

Werner Wiedenamann presented the results of his benchmarking and Athena optimizatiuon work at the July ATLAS TDAQ week. Although the instrumentation of the Athena software is a cumbersome and time-consuming process, the understanding gained so far makes the whole effort worthwhile. During the TDAQ week and in a subsequent phone meeting, discussions were held with members of the Barcelona group in order to coordinate the work leading to the full instrumentation of Athena. After these meetings, W.Wiedenmann released his instrumentation tools (via web). The plan is to start benchmarking, including the data conversion services, at the end of August.

Work is continuing (with ANL) on drafting a note summarizing design ideas and issues on LVL2 trigger prescaling and LVL2 Detailed result.